

MAINTENANCE CARD



ODT COMMANDS

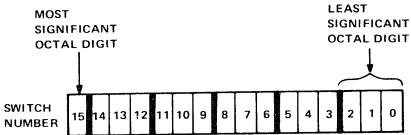
Format	Description
(CR)	Close opened location; accept next command.
(LF)	Close current location; open next sequential location, or GPR.
↑ or Λ	Open previous location or GPR.
← or _	Take contents of opened location, index by contents of PC, and open that location.
@	Take contents of opened location as absolute address and open that location.
r/	Open the word at location r.
/	Reopen the last location.
\$n/ or Rn/	Open general register n (0-7) or S (PS register).
r;G or rG	Go to location r and start program.
nL	Execute bootstrap loader using n as device CSR. Console device address is 177560.
;P or P	Proceed with program execution.
RUBOUT/ DELETE	Erases previous numeric character. Response is a backslash (\).
M	Print internal register contents. Data indicates how CPU entered ODT.
	<u>XXXXXXN</u> where:
	N = 0 or 4 Halt instruction on B Halt line.
	1 or 5 Bus error while getting device interrupt vector.
	2 or 6 Bus error during memory refresh.
	3 Double bus error (stack contains non-existent address).
	4 Reserved instruction trap.
	7 Conditions 1, 2, 4 occurred.

In order for valid data to be displayed following an error condition, this command must be executed immediately.

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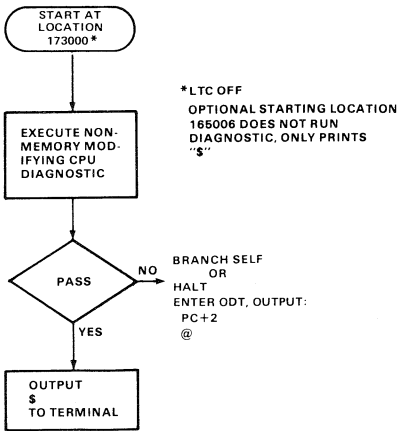
SWITCH REGISTER TO OCTAL CONVERSION



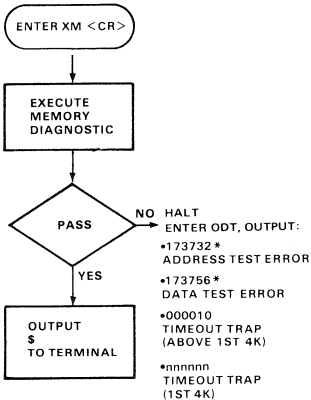
SWITCH X UP	=	OCTAL
0	—	1
1	—	2
2	—	4
3	—	10
4	—	20
5	—	40
6	—	100
7	—	200
8	—	400
9	—	1000
10	—	2000
11	—	4000
12	—	10000
13	—	20000
14	—	40000
15	—	100000

REV11 COMMANDS AND DIAGNOSTICS (M9400)

REV11 STARTUP FLOWCHART

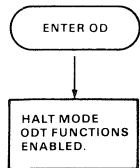


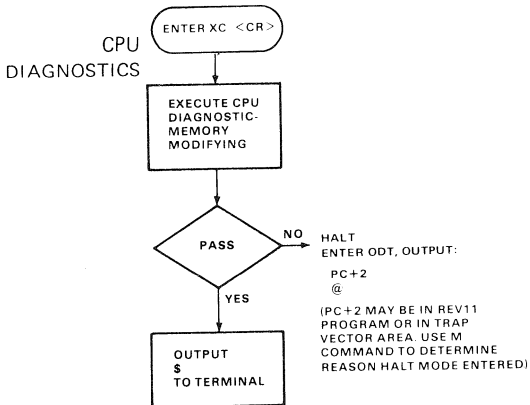
MEMORY DIAGNOSTIC



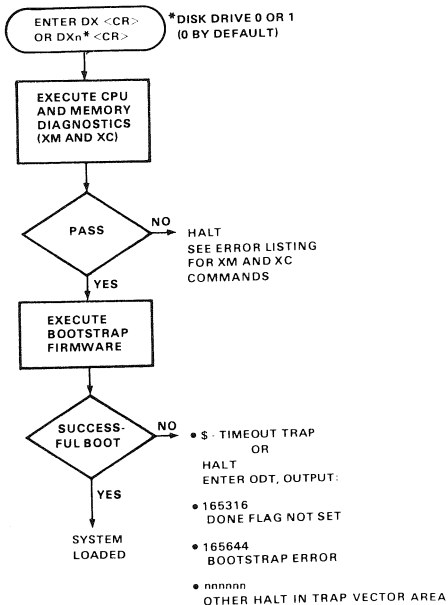
* GOOD DATA -R3
 BAD DATA -ADDRESS R2

ODT

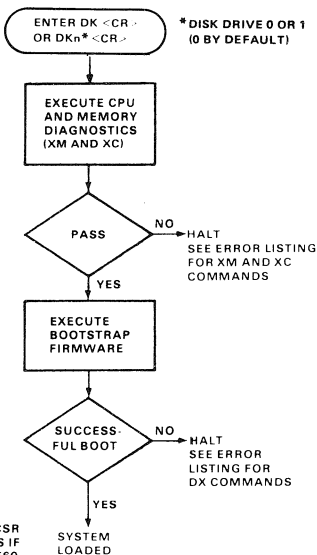




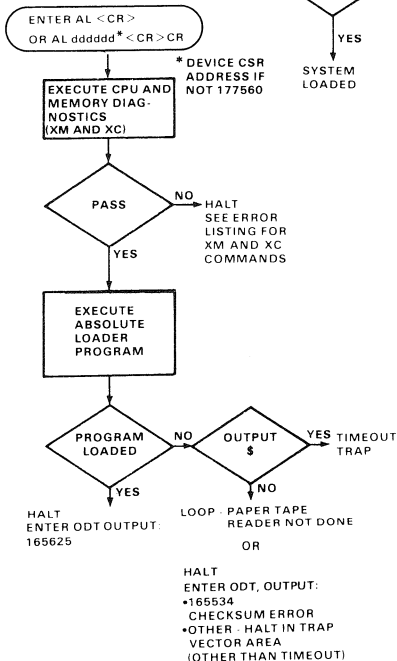
RXV11 BOOTSTRAP



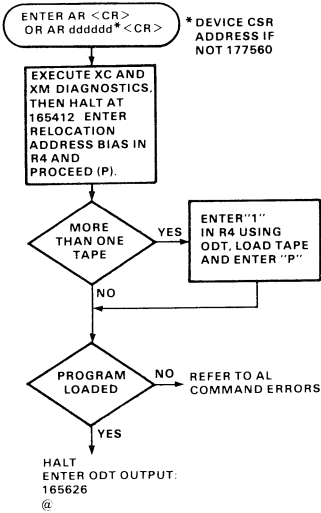
RK05 BOOTSTRAP



ABSOLUTE LOADER



ABSOLUTE LOADER (RELOCATED)

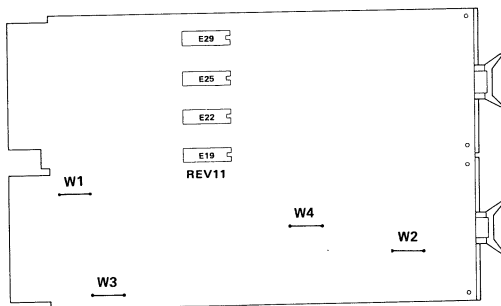


MODULE VERSIONS AND JUMPERS

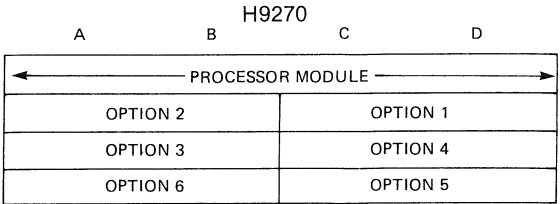
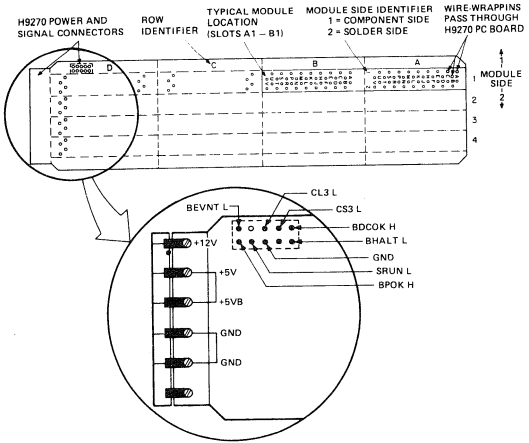
MODULE # M9400 -	120 Ω TERM	250 Ω TERM	BOOT & DIAG. ROMS	DMA REFRESH	CABLE CONN	W1 BDMG	W2 REFRESH ENABLE	W3 (FACTORY)	W4 ROM ENABLE	OPTION
YA *	Solid	Solid	Solid	Solid	X	X	X	X	X	REV 11-A
YB	Solid	Solid	Solid	Solid	X	X	X	X	X	TEV11 (TERM.)
YC *	Solid	Solid	Solid	Solid	X	X	X	X	X	REV11-C
YD	Solid	Solid	Solid	Solid	X	X	X	X	X	CABLE CONN.
YE	Solid	Solid	Solid	Solid	X	X	X	X	X	CABLE CONN. W/TERM
YF *	Solid	Solid	Solid	Solid	X	X	X	X	X	REV11-F
YH *	Solid	Solid	Solid	Solid	X	X	X	X	X	REV11-H **
YJ *	Solid	Solid	Solid	Solid	X	X	X	X	X	REV11-J

TABLE SHOWS STANDARD JUMPERS (X = INSERT)
(SOLID = MODULE FUNCTIONS)

*FACTORY SET POTENTIOMETER ** REMOTE BOOT



H9270 PIN IDENTIFICATION



NOTE 1. Unused slots require backplane jumpers for
 BIAKI/O L
 BDMGI/O L

BACKPLANES (Cont.)

DDV11-B

A	B	C	D	E	F	
← PROCESSOR →						1
	OPTION 2		OPTION 1			2
	OPTION 3		OPTION 4			3
	OPTION 6		OPTION 5			4
	OPTION 7		OPTION 8			5
	OPTION 10		OPTION 9			6
	OPTION 11		OPTION 12			7
	OPTION 14		OPTION 13			8
	OPTION 15		OPTION 16			9

} USER DEFINED SLOTS

NOTE 1. Unused slots require backplane jumpers for
 BIAKI/O L
 BDMGI/O L

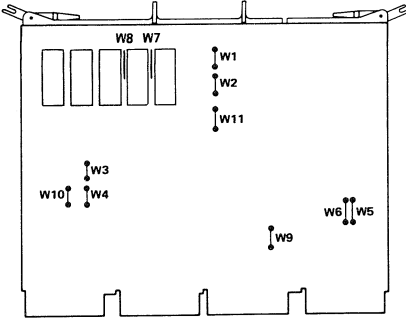
NOTE 2. A terminator is required in the last unused option slot if 7 to 15 unit loads are installed. (One module = one unit load.)

MULTIPLE BACKPLANE CONFIGURATION

NUMBER OF H9270 BACKPLANES	BACKPLANE OPTION		
	BCV1B-XX*	BCV1A-XX*	
	1st to 2nd	2nd to 3rd	3rd
2	M9400-YE to M9401	terminate first unused option slot	_____
3	M9400-YE to M9401	M9400-YD to M9401	terminate first unused option slot

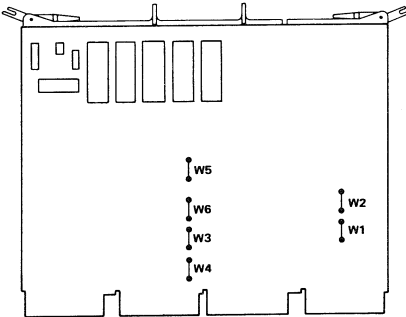
*NOTE: XX denotes cable length. BCV1B-XX and BCV1A-XX cables in a 3 backplane system must differ by at least four feet.

KD11 PROCESSOR (M7264)



ALL JUMPERS (EXCEPT 7 AND 8) ARE WIRE WRAPPED.

M7264 ETCH REV E (AND LATER)



ALL JUMPERS ARE WIRE-WRAPPED.

M7264 ETCH REV C, D (W7-W11 NOT USED)

OPTION IDENTIFICATION

	NO EIS/FIS	EIS/FIS	DIBOL/EIS
NO MOS	KD11-H	KD11-N	KD11-Q
MOS	KD11-F	KD11-L	KD11-P

KD 11 PROCESSOR (Cont.)

ALL ETCH REV (JUMPERS)

RESIDENT MEMORY ADDRESSING

(N/A KD11-H, N)

Bank	W1	W2
0	R	I
1	I	R
Not addressed	R	R

LTC EXTERNAL

	W3
Enable	R
Disable	I

PROCESSOR REFRESH

	W4
Enable	R
Disable	I

POWER UP

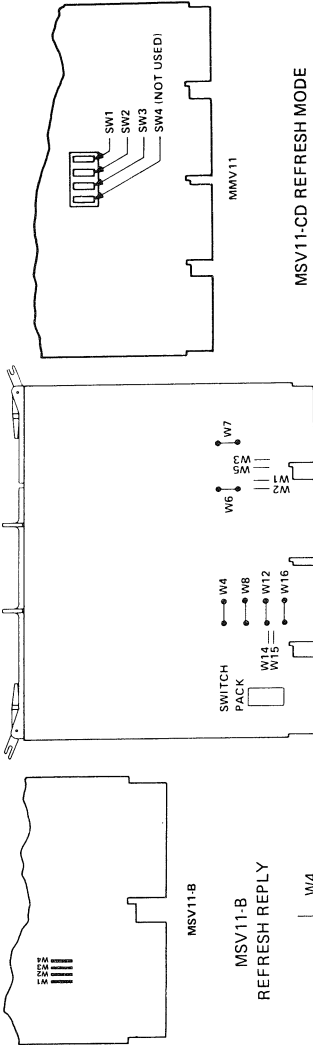
MODE	W5	W6
0—to 24	R	R
1—to ODT	I	R
2—to 173000	R	I
3—to special	I	I

Potentiometer – Factory Set

ETCH REV E AND ABOVE ONLY (JUMPERS)

	Jumper	Enable	Disable
BIAS VOLTAGE	W7, W8	FACTORY	FACTORY
ON-BOARD PROCESSOR MEMORY			
REPLY	W9	R	I
REFRESH REPLY	W10	R	I
MEMORY SELECT	W11	I	R

MSV11-B M7944
 MSV11-CD M7955
 MMV11-A G653/H223



	W6	W7	W6	W7
Internal Refresh	Reply Enable	Reply Enable	Reply Enable	Reply Enable
External Refresh	Illegal	R	I	R

NOTE: Memory requiring refresh that is electrically furthest from refresh signals returns refresh reply. All others are disabled.

CORE AND MOS
MEMORY STARTING ADDRESS SWITCHES AND JUMPERS

MSV11-B JUMPER			MSV11-CD SWITCH*			MMV11-A SWITCH				BANK	STARTING ADDRESS
W1	W2	W3	S1	S2	S3	SW4	SW3	SW2	SW1		
I	I	I	O	O	O	-	O	O	O	0	0
I	I	R	F	O	O	-	O	O	F	1	20000
I	R	I	O	F	O	-	O	F	O	2	40000
I	R	R	F	F	O	-	O	F	F	3	60000
R	I	I	O	O	F	-	F	O	O	4	100000
R	I	R	F	O	F	-	F	O	F	5	120000
R	R	I	O	F	F	-	F	F	O	6	140000
I/O PAGE			I/O PAGE						I/O PAGE	7	160000

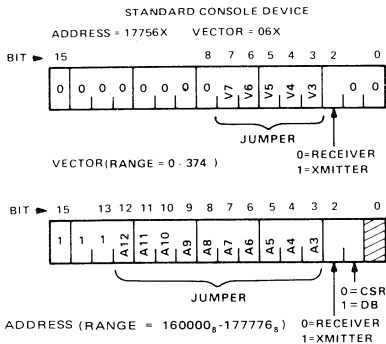
*Switches 4 and 5 always on

SWITCHES 4 AND 5 ALWAYS ON
I = JUMPER INSERTED O = SWITCH ON
R = JUMPER REMOVED F = SWITCH OFF

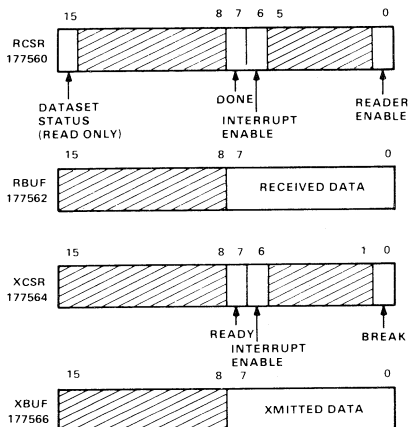
MSV11-CD MEMORY SIZE

SIZE	W4	W8	W12	W16
16K	I	I	I	I
12K	I	I	I	R
8K	I	I	R	R
4K	I	R	R	R

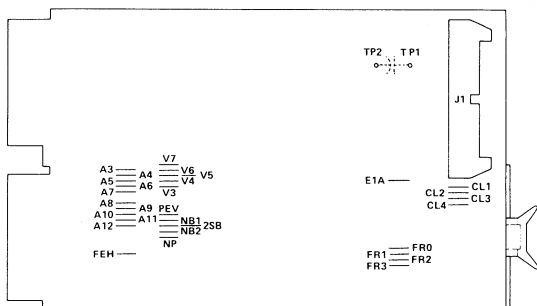
W1, 2, 3, and 5-Battery Backup, see MSV11-CD in Microcomputer Handbook (2nd edition) W14, 15-Bus Continuity, Factory Set. (installed)



ALL JUMPERS REMOVE = 1 INSERT = 0



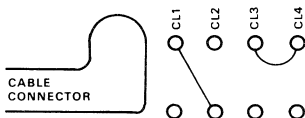
DLV11 (Cont.)



XMIT/RECEIVE MODE

CURRENT LOOP Active: CL 1, 2, 3, 4 ALL INSERTED

Passive:



BAUD RATE: XMIT/REC

BAUD RATE	FR—				BAUD RATE	FR—			
	0	1	2	3		0	1	2	3
50	I	R	I	I	600	I	R	R	I
75	I	I	I	I	1200	R	R	I	R
110	R	R	R	R	1800	I	R	I	R
134.5	I	I	R	I	2400	R	R	R	I
150	I	R	R	R		I	I	R	R
200	R	I	R	I	4800	R	I	I	R
300	R	I	R	R	9600	I	I	I	R
					EXT (PIN BH1)	—	I	I	R

DLV11 (Cont.)

PARITY			BREAK	
	PEV	NP		FEH
ENABLE odd	I	I	ENABLE	I
even	R	I	DISABLE	R
DISABLE	-	R		

DATA FORMAT				
No. of Data Bits	NB1	NB2	No. of Stop Bits	2Sb
5	I	I	1	I
6	R	I	2	R
7	I	R		
8	R	R		

- NOTE:
- FOR LT33 (ASR33) or LT35 (ASR35) insert 0.005 μ f capacitor between TP1-TP2.
 - EIA CABLE – BCO5C-X
 - 20 mA CURRENT LOOP CABLE – BCO5M-X

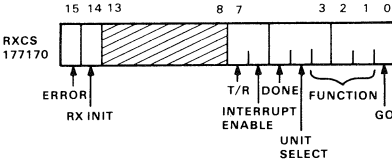
RXCS

COMMAND FUNCTIONS

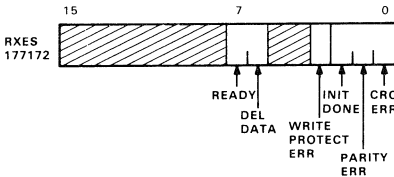
COMMAND PROTOCOL

Function	Command	Protocol
Full Buffer	000	1. Issue function and GO.
Empty Buffer	001	2. Wait for done.
Write Sector	010	3. Check buffer for status.
Read Sector	011	
Not used	100	Read Definitive Error Code
Read Status	101	1. Issue functions and GO.
Write Sector with deleted data	110	2. Wait for done.
Read Error Code	111	3. Check buffer for definitive errors.

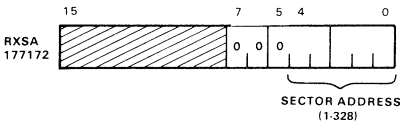
CONTROL STATUS REGISTER



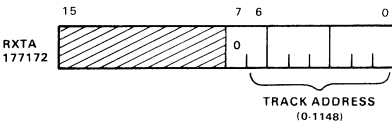
ERROR AND STATUS REGISTER



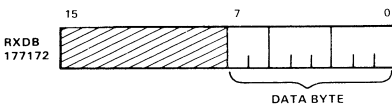
SECTOR ADDRESS REGISTER



TRACK ADDRESS REGISTER



DATA BUFFER REGISTER



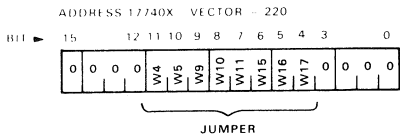
ERROR CODES AND MEANINGS

0010 /DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
0020 DRIVE 1 FAILED TO SEE HOME ON INITIALIZE
0030 /FOUND HOME WHEN STEPPING OUT 10 TRACKS FOR
INIT
0040 /TRIED TO ACCESS A TRACK GREATER THAN 76
0050 /HOME FOUND BEFORE DESIRED TRACK WAS
REACHED
0060 /SELF-DIAGNOSTIC ERROR
0070 /DESIRED SECTOR COULD NOT BE FOUND AFTER
/LOOKING AT 52 HEADERS
0100 /WRITE COMMAND ON A WRITE PROTECTED DISK
0110 /MORE THAN 40 MICROSEC AND NO SEP CLOCK SEEN
0120 /A PREAMBLE COULD NOT BE FOUND
0130 /PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN
/ALLOWABLE TIME SPAN
0140 /CRC ERROR ON A HEADER, NO FLAG
0150 /THE HEADERS TRACK ADDRESS OF A GOOD HEADER
/DOES NOT COMPARE WITH THE DESIRED TRACK
0160 /TOO MANY TRIES FOR A ID ADDRESS MARK
0170 /DATA MARK NOT FOUND IN ALLOTTED TIME
0200 /CRC ERROR ON READING THE SECTOR FROM THE
DISK
0210 /PARITY ERROR ON SOME WORD FROM INTERFACE

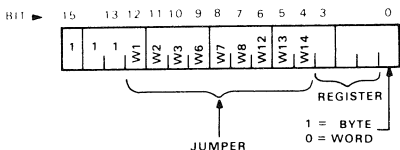
RXV11 BOOTSTRAP (Drive 0 only)
(terminal response underlined)

START: @001000/000000 5000 <LF>
001002/000000 12701 <LF>
001004/000000 177170 <LF>
001006/000000 105711 <LF>
001010/000000 1776 <LF>
001012/000000 12711 <LF>
001014/000000 3 <LF>
001016/000000 5711 <LF>
001020/000000 1776 <LF>
001022/000000 100405 <LF>
001024/000000 105711 <LF>
001026/000000 100004 <LF>
001030/000000 116120 <LF>
001032/000000 2 <LF>
001034/000000 770 <LF>
001036/000000 0 <LF>
001040/000000 5007 <LF>
001042/000000 0 <CR>

STANDARD DEVICE

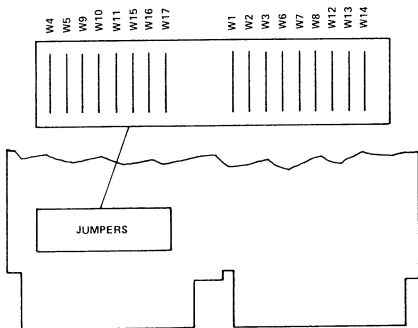


VECTOR (RANGE 0-7760)



ADDRESS (RANGE 160000 - 177777)

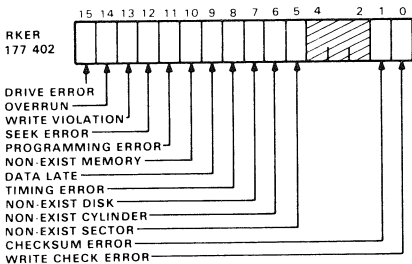
ALL JUMPERS REMOVE = "0" INSERT = "1"



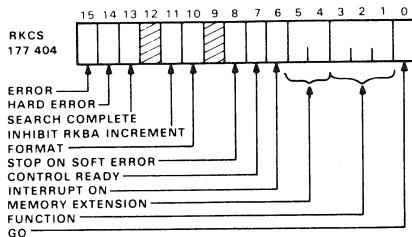
RKV11

RKV11 (Cont.)

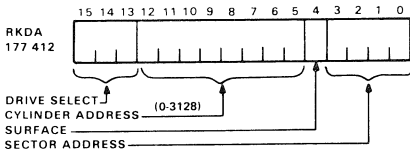
ERROR REGISTER



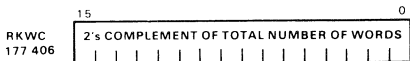
CONTROL STATUS REGISTER



DISK ADDRESS REGISTER

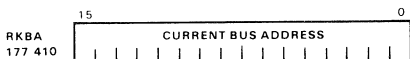


WORD COUNT REGISTER

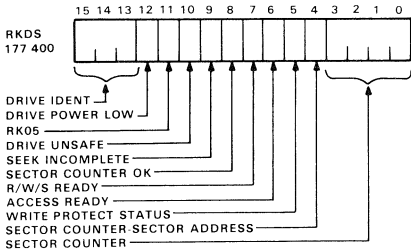


MI-0706

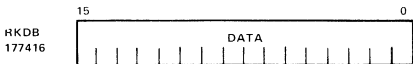
CURRENT BUS ADDRESS REGISTER



DRIVE STATUS REGISTER



DATA BUFFER REGISTER



RKV11 BOOTSTRAP (Drive 0 only)
(terminal response underlined)

```

START  @001000/000000 5<LF>
        001002/000000 10061<LF>
        001004/000000 6<LF>
        001006/000000 12761<LF>
        001010/000000 177400<LF>
        001012/000000 2<LF>
        001014/000000 12711<LF>
        001016/000000 5<LF>
        001020/000000 105711<LF>
        001022/000000 100376<LF>
        001024/000000 5007<LF>
        001026/000000 0<CR>
        @R0/XXXXXX 0<LF>
        R1/XXXXXX 177404<CR>
    
```


JUMPER CONFIGURATION

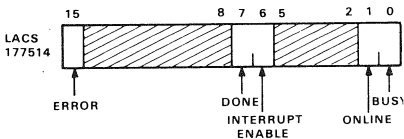
Jumper	LA180 ¹	Centronics ²
W1	I	I
W2	I	R
W3	R	I
W4	R	R
W5	I	I
W6	R	R
W7	I	I

I = Insert R = Remove

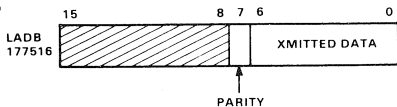
¹ Models 101, 101A, 101D, 102A, 303.

² CAUTION – The LA180 will not function unless jumper W6 on the LA180 logic board is installed; the interface cable must be installed with P1 to the interface and P2 to the printer.

CONTROL AND STATUS REGISTER

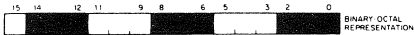


DATA BUFFER REGISTER



LSI-11 INSTRUCTION SET

WORD FORMAT



Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2= $\%02$]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is addr; (R) + (1 or 2)
3	auto-incr deferred	$\% (R)+$	(R) is adrs of adrs; (R) + 2
4	auto-decrement	-(R)	(R) - (1 or 2); is adrs
5	auto-decr deferred	$\% -(R)$	(R) - 2; (R) is adrs of adrs
6	index	X(R)	(R) + X is adrs
7	index deferred	$\% X(R)$	(R) + X is adrs of adrs

PROGRAM COUNTER ADDRESSING

Reg = 7

Mode	Name	Symbolic	Description
2	immediate	#n	operand n follows instr
3	absolute	$\% \#A$	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

LEGEND

Op Codes

- = 0 for word/1 for byte
- SS = source field (6 bits)
- DD = destination field (6 bits)
- R = gen register (3 bits), 0 to 7
- XXX = offset (8 bits), +127 to -128
- N = number (3 bits)
- NN = number (6 bits)

Boolean

- ∧ = AND
- ∨ = inclusive OR
- ⊖ = exclusive OR
- ¬ = NOT

Operations

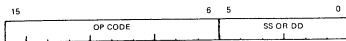
- () = contents of
- s = contents of source
- d = contents of destination
- r = contents of register
- ← = becomes
- X = relative address
- $\%$ = register definition

Condition Codes

- * = conditionally set/cleared
- = not affected
- 0 = cleared
- 1 = set

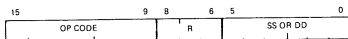
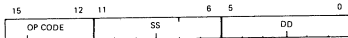
LSI-11 INSTRUCTION SET (Cont.)

SINGLE OPERAND: OPR dst



Mnemonic	Op Code	Instruction	dst Result	N	Z	V	C
General							
CLR(B)	050DD	clear	0	0	1	0	0
COM(B)	051DD	complement (1's)	$\sim d$	*	*	0	1
INC(B)	052DD	increment	$d + 1$	*	*	*	-
DEC(B)	053DD	decrement	$d - 1$	*	*	*	*
NEG(B)	054DD	negate (2's compl)	$-d$	*	*	*	*
TST(B)	057DD	test	d	*	*	0	0
Rotate & Shift							
ROR(B)	060DD	rotate right	$\rightarrow C, d$	*	*	*	*
ROL(B)	061DD	rotate left	$C, d \leftarrow$	*	*	*	*
ASR(B)	062DD	arith shift right	$d/2$	*	*	*	*
ASL(B)	063DD	arith shift left	$2d$	*	*	*	*
SWAB	0003DD	swap bytes		*	*	0	0
Multiple Precision							
ADC(B)	055DD	add carry	$d + C$	*	*	*	*
SBC(B)	056DD	subtract carry	$d - C$	*	*	*	*
SXT	0067DD	sign extend	0 or -1	-	*	0	-
Processor Status (PS) Operators							
MFPS	1067DD	move byte from PS	$d \leftarrow PS$	*	*	0	-
MTPS	1064SS	move byte to PS	$PS \leftarrow s$	*	*	*	*

DOUBLE OPERAND: OPR src, dst OPR src, R or OPR R, dst



Mnemonic	Op Code	Instruction	Operation	N	Z	V	C
General							
MOV(B)	1SSDD	move	$d \leftarrow s$	*	*	0	-
CMP(B)	2SSDD	compare	$s - d$	*	*	*	*
ADD	06SSDD	add	$d \leftarrow s + d$	*	*	*	*
SUB	16SSDD	subtract	$d \leftarrow d - s$	*	*	*	*
Logical							
BIT(B)	3SSDD	bit test (AND)	$s \wedge d$	*	*	0	-
BIC(B)	4SSDD	bit clear	$d \leftarrow (\sim s) \wedge d$	*	*	0	-
BIS(B)	5SSDD	bit set (OR)	$d \leftarrow s \vee d$	*	*	0	-
XOR	074RDD	exclusive OR	$d \leftarrow r \vee d$	*	*	0	-

LSI-11 INSTRUCTION SET (Cont.)

Optional EIS

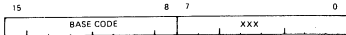
MUL	070RSS	multiply	$r \leftarrow r \times s$	* * 0 *
DIV	071RSS	divide	$r \leftarrow r/s$	* * * *
ASH	072RSS	shift		* * * *
		arithmetically		* * * *
ASHC	073RSS	arith shift		* * * *
		combined		* * * *

Optional FIS

FADD	07500R	floating add		* * 0 0
FSUB	07501R	floating subtract		* * 0 0
FMUL	07502R	floating multiply		* * 0 0
FDIV	07503R	floating divide		* * 0 0

BRANCH: B -- location

If condition is satisfied:
Branch to location,
New PC \leftarrow Updated PC + (2 x offset)
 $\underbrace{\hspace{10em}}_{\text{adrs of br instr} + 2}$



Op Code = Base Code + XXX

Mne- monic	Base Code	Instruction	Branch Condition
---------------	-----------	-------------	------------------

Branches

BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	$\neq 0$	Z = 0
BEQ	001400	br if equal (to 0)	$= 0$	Z = 1
BPL	100000	branch if plus	$\neq -$	N = 0
BMI	100400	branch if minus	$-$	N = 1
BVC	102000	br if overflow is clear		V = 0
BVS	102400	br if overflow is set		V = 1
BCC	103000	br if carry is clear		C = 0
BCS	103400	br if carry is set		C = 1

Signed Conditional Branches

BGE	002000	br if greater or equal (to 0)	≥ 0	$N \neq V = 0$
BLT	002400	br if less than (0)	< 0	$N \neq V = 1$
BGT	003000	br if greater than (0)	≥ 0	$Z \vee (N \neq V) = 0$
BLE	003400	br if less or equal (to 0)	≤ 0	$Z \vee (N \neq V) = 1$

Unsigned Conditional Branches

BHI	101000	branch if higher	\geq	$C \vee Z = 0$
BLOS	101400	branch if lower or same	\leq	$C \vee Z = 1$
BHIS	103000	branch if higher or same	\geq	C = 0
BLO	103400	branch if lower	$<$	C = 1

LSI-11 INSTRUCTION SET (Cont.)

JUMP & SUBROUTINE

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	} use same R
RTS	00020R	return from subroutine	
MARK	0064NN	mark	aid in subr return
SOB	077RNN	subtract 1 & br (if ≠ 0)	(R) - 1, then if (R) ≠ 0: PC ← Updated PC - (2 x NN)

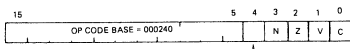
TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)

CONDITION CODE OPERATORS:



0 = CLEAR SELECTED COND. CODE BITS
1 = SET SELECTED COND. CODE BITS

Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	clear C	-	-	-	0
CLV	000242	clear V	-	-	0	-
CLZ	000244	clear Z	-	0	-	-
CLN	000250	clear N	0	-	-	-
CCC	000257	clear all cc bits	0	0	0	0
SEC	000261	set C	-	-	-	1
SEV	000262	set V	-	-	1	-
SEZ	000264	set Z	-	1	-	-
SEN	000270	set N	1	-	-	-
SCC	000277	set all cc bits	1	1	1	1

LSI-11 INSTRUCTION SET (Cont.)

NUMERICAL OP CODE LIST

OP Code	Mnemonic	OP Code	Mnemonic	OP Code	Mnemonic	
00 00 00	HALT	00 60 DD	ROR	10 40 00	} EMT	
00 00 01	WAIT	00 61 DD	ROL	↓		
00 00 02	RTI	00 62 DD	ASR	↓		
00 00 03	BPT	00 63 DD	ASL	10 43 77		
00 00 04	IOT	00 64 NN	MARK	10 44 00	} TRAP	
00 00 05	RESET	00 67 DD	SXT			↓
00 00 06	RTT	00 70 00	} (unused)	10 47 77		
00 00 07	} (unused)			↓		
00 00 77			00 77 77		10 50 DD	CLRB
00 01 DD	JMP	01 SS DD	MOV	10 51 DD	COMB	
00 02 0R	RTS	02 SS DD	CMP	10 52 DD	INCB	
00 02 10	} (reserved)	03 SS DD	BIT	10 53 DD	DECB	
		04 SS DD	BIC	10 54 DD	NEGB	
		05 SS DD	BIS	10 55 DD	ADCB	
		06 SS DD	ADD	10 56 DD	SBCB	
00 02 40	NOP	07 0R SS	MUL	10 57 DD	TSTB	
00 02 41	} cond codes	07 1R SS	DIV	10 60 DD	RORB	
		07 2R SS	ASH	10 61 DD	ROLB	
		07 3R SS	ASHC	10 62 DD	ASRB	
		07 4R DD	XOR	10 63 DD	ASLB	
00 02 77				10 64 SS	MTPS	
				10 67 DD	MFPS	
00 03 DD	SWAB	07 50 0R	FADD	11 SS DD	MOVB	
00 04 XXX	BR	07 50 1R	FSUB		12 SS DD	CMPB
00 10 XXX	BNE	07 50 2R	FMUL		13 SS DD	BITB
00 14 XXX	BEQ	07 50 3R	FDIV		14 SS DD	BICB
00 20 XXX	BGE	07 50 40	} (unused)	15 SS DD	BISB	
00 24 XXX	BLT			16 SS DD	SUB	
00 30 XXX	BGT	↓		17 00 00	} RE-SERVED	
00 34 XXX	BLE	07 67 77				↓
00 4R DD	JSR	07 7R NN	SOB	17 77 77		
00 50 DD	CLR	10 00 XXX	BPL			
00 51 DD	COM	10 04 XXX	BMI			
00 52 DD	INC	10 10 XXX	BHI			
00 53 DD	DEC	10 14 XXX	BLOS			
00 54 DD	NEG	10 20 XXX	BVC			
00 55 DD	ADC	10 24 XXX	BVS			
00 56 DD	SBC	10 30 XXX	BCC,			
00 57 DD	TST		BHIS			
		10 34 XXX	BCS,			
			BLO			

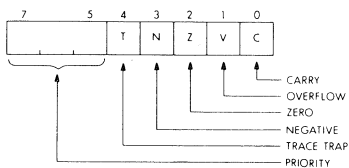
RESERVED TRAP AND INTERRUPT VECTORS

000	(Reserved)	030	EMT Instruction
004	Bus Timeout and Illegal Instructions (eg. JMP R0) (Odd Address and Stack Overflow Traps Not Implemented on LSI-11)	034	TRAP Instruction
		060	Console Input Device
		064	Console Output Device
		100	External Event Line Interrupt
010	Illegal and Reserved Instruction	200	LAV11
		244	FIS (Optional)
014	BPT Instruction and T Bit	264	RXV11
020	IOT Instruction	300	Floating Vectors start here
024	Power Fail		

7-BIT ASCII CODE

Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
000	NUL	040	SP	100	W	140	\
001	SOH	041	!	101	A	141	a
002	STX	042	..	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	\$	104	D	144	d
005	ENO	054	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	.	107	G	147	g
010	BS	050	(110	H	150	h
011	HT	051)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[173	{
034	FS	074	<	134	\	174	
035	GS	075	=	135] or ^	175	}
036	RS	076	>	136	^ or _	176	~
037	US	077	?	137	- or ←	177	DEL

PROCESSOR STATUS WORD



LSI-11 BUS PINNING

Row A (Same as Row C)		Row B (Same as Row D)	
Module Side 1 (Component Side)			
AA1	BSPARE1	BA1	BDCOK H
AB1	BSPARE2	BB1	BPOK H
AC1	BAD16	BC1	SSPARE4
AD1	BAD17	BD1	SSPARE5
AE1	SSPARE1	BE1	SSPARE6
AF1	SSPARE2	BF1	SSPARE7
AH1	SSPARE3	BH1	SSPARE8
AJ1	GND	BJ1	GND
AK1	MSPARE A	BK1	MSPARE B
AL1	MSPARE A	BL1	MSPARE B
AM1	GND	BM1	GND
AN1	BDMR L	BN1	BSACK L
AP1	BHALT L	BP1	BSPARE6
AR1	BREF L	BR1	BEVNT L
AS1	PSPARE3	BS1	PSARE4
AT1	GND	BT1	GND
AU1	PSPARE1	BU1	PSPARE2
AV1	+5B	BV1	+5
Module Side 2 (Solder Side)			
AA2	+5	BA2	+5
AB2	-12	BB2	-12
AC2	GND	BC2	GND
AD2	+12	BD2	+12
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	BWTTB L	BK2	BDAL6 L
AL2	BIRO L	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDAL0 L	BU2	BDAL14 L
AV2	BDAL1 L	BV2	BDAL15 L

NOTES:

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EQUIPMENT
CORPORATION

MAYNARD, MASSACHUSETTS

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