PDP-11/05,11/10 computer manual

digital

EK-11005-TM-003

PDP-11/05,11/10
computer manual

digital equipment corporation · maynard. massachusetts

1st Edition, February 1973
2nd Printing, September 1973
3rd Printing, July 1974
4th Printing, September 1974
2nd Edition, April 1975

Printed in U.S.A.

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FOREWORD

This manual describes the PDP-11/05 and PDP-11/10 Computers. The PDP-11/05 and PDP-11/10 are electrically identical. The PDP-11/05 is specified for the Original Equipment Manufacturer (OEM) market and the PDP-11/10 is specified for the end user market.

The PDP-11/05 is available in two versions: one provides a maximum of 8K words of core memory and the other provides a maximum of 16K words of core memory. The PDP-11/10 is available only with a maximum of 8K words of core memory.

This manual is divided into four parts.

Part 1	Computer Description
Part 2	KD11-B Processor
Part 3	MM11-K, MM11-L Memories
Part 4	Power Supply

Chapter outlines of each part are shown below.

Part 1 COMPUTER DESCRIPTION

Chapter 1	Computer Components
Chapter 2	Unibus
Chapter 3	Unpacking and Installation
Chapter 4	Operation

Part 2 KD11-B PROCESSOR

Chapter 5	Processor General Description
Chapter 6	Instruction Set
Chapter 7*	Console Description
Chapter 8*	KD11-B Detailed Description
Chapter 9*	Microprogram Control
Chapter 10*	KD11-B and Console Maintenance

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Chapter 11	MM11-K and L General Description
Chapter 12	MM11-K and L Detailed Description
Chapter 13	Memory Maintenance

*Chapters 7, 8, 9, and 10 have been deleted. Current information is available in the KD11-B Processor Maintenance Manual.

Part 4 POWER SUPPLY

Chapter 14	Power Supply General Description
Chapter 15	Power Supply Detailed Description
Chapter 16	Power Supply Maintenance

Part 5 10-1/2 INCH MOUNTING BOX AND POWER SUPPLY

Chapter 17	Mounting Box
Chapter 18	Unpacking and Installation
Chapter 19	Power System

A bound volume of engineering drawings is supplied with each computer.

The following related documents are valuable as references.

PDP-11/05, 11/10 Processor Handbook
PDP-11 Peripherals Handbook
PDP-11 Paper-Tape Software Programming Handbook
(Document No. DEC-11-GGPB-D)

PART 1

COMPUTER DESCRIPTION

Part 1 provides a general physical description of the PDP-11/05 and PDP-11/10 computers. Unibus operation is discussed prior to the discussions of computer installation and operation. The chapters of Part 1 are:

Chapter 1 – Computer Components
Chapter 2 – Unibus
Chapter 3 – Unpacking and Installation
Chapter 4 – Operation

CHAPTER 1
COMPUTER COMPONENTS

1.1 INTRODUCTION

This chapter briefly describes the major components of the PDP-11/05, 11/10 Computer. It includes module utilization diagrams for both computer configurations and a backplane connector and pin designation diagram.

1.2 COMPUTER COMPONENTS

The computer consists of a mounting box, console, processor, core memory, prewired backplane, power supply, fans, and interconnecting cables. The processor is contained on two modules, and each 4K or 8K memory is contained on three modules.

1.2.1 KD11-B Processor

The processor comprises the M7260 Data Path Module and the M7261 Control Logic and Microprogram Module. They are hex height modules which measure 8-1/2 inches long by 15 inches high. A hex height module contains six edge connectors (A-F).

All the processor functional components are contained on these modules. The M7260 Data Path Module contains: data path logic, processor status word logic, auxiliary arithmetic logic unit control, instruction register and decoding logic, and serial communications line interface. The M7261 Control Logic and Microprogram Module contains: internal address detecting logic, stack control logic, Unibus control logic, priority arbitration logic, Unibus drivers and receivers, microbranch logic, microprogram counter, control store logic, power fail logic, line clock, and processor clock.

The serial communications line (SCL) interface is directly connected to the desired serial communications device. It can operate at speeds of 110–300 baud and is program compatible with the KL11 Teletype Control Interface option. The SCL is compatible with the LA30 DECwriter at 30 characters per second, the VT05 Alphanumeric CRT Display Terminal at 30 characters per second, and the Teletype Model 33 ASR at 10 characters per second.

The line time clock (LTC) allows the program to measure time by sensing the 50 Hz or 60 Hz ac line frequency. This clock is program compatible with the KW11-L Line Time Clock option.

The line time clock and the serial communications line interface are not connected to the Unibus; they use an internal bus and can be addressed only by the processor and the console.

1.2.2 Core Memory

The PDP-11/05 is available in two versions: one provides a maximum of 8K words of core memory and the other provides a maximum of 16K words. The PDP-11/10 is available only with a maximum of 8K words of core memory. A separate add-on core memory system (ME11-L) is available to provide an additional 8K, 16K, or 24K words of core memory. A PDP-11/05 or PDP-11/10 processor provides program control for a maximum of 32K words of memory; therefore, the self-contained memory plus the ME11-L must not be greater than 32K words.

1.2.2.1 Memory Organization – The memory is organized in 16-bit words consisting of two 8-bit bytes. The bytes are identified as low and high. The memory contains 8192 words or 16,384 bytes; therefore, 16,384 locations are assigned. The address locations are specified as 6-digit octal numbers. The 16,384 locations for the 8K memory are designated 000000 through 037777.

Each byte is addressable and has its own address location; low bytes are even numbered and high bytes are odd numbered. Words are addressed at even numbered locations only, and the high (odd) byte is automatically included. Consecutive words are therefore found in even numbered addresses.

The PDP-11 address word contains 18 bits [A (17:00)], which provides the capability of addressing 262,144 (256K) locations (bytes) or 131,072 (128K) words. The basic processor provides 16 bits [A (15:00)] of address information, which handles 65,536 (64K) bytes or 32,768 (32K) words. During an addressing operation, if bits A (15:13) are all 1s, bits A (17:16) are forced to 1s, which relocates the last 8K bytes (4K words) to become the highest locations accessed by the bus. These top 4,096 word locations are reserved for peripheral and register addresses, and the user therefore has 28,672 (28K) words of memory to program.

1.2.2.2 Memory Specification – The core memory is a read/write, random access, coincident current type with a cycle time of 900 ns and an access time of 400 ns. It is organized in a 3-dimensional, 3-wire planar configuration with a word length of 16 bits. The memory is offered in two word capacities: the MM11-K Core Memory contains 4096 words and the MM11-L Core Memory contains 8192 words. Each memory is contained on three modules designated the stack, control, and driver modules. For the MM11-K memory, the stack module is H213; H214 is the stack module for the MM11-L memory. The G110 Control Module and the G231 Driver Module are the same for both memories.

1.2.3 Power Supply

The power supply consists of a dc regulator module, transformer, and fan, mounted in a chassis. It is installed in the computer mounting box. The power supply converts 115V or 230V, 47-63 Hz line voltage to three regulated dc voltages that are used by the processor, memory, and optional modules. The regulated voltages are: +5V at 17A, -15V at 6A, and +15V at 1A.

An associated component, the power control, provides the ac line voltage to the power supply and cooling fans. The power control is installed in the rear panel of the computer mounting box. It consists of a line cord, circuit breaker, and output connector. A model is available for each of the two line voltages (115V or 230V), as shown below.

Power Control Part Number	Rating
BC05H	7A at 115V/47-63 Hz
BC05J	4A at 230V/47-63 Hz

The power supply provides three additional outputs. Signal LTC L is the Line Time Clock signal that drives the line time clock. The BUS AC LO L and BUS DC LO L signals actuate the processor power-fail auto-restart circuitry.

1.2.4 Backplane

The backplane is the connector assembly into which the computer modules are plugged. It provides interconnections between the Unibus, processor, memory, and optional modules. The interconnections are made via a printed circuit board and wirewrapped pins that are part of the backplane assembly.

The backplane is wired differently for the 8K and 16K memory versions of the computer. As a result, the modules must be installed in specific locations as shown in Figure 1-1 for the 16K version and Figure 1-2 for the 8K version. These illustrations show the backplane as viewed from the module side. The slots are numbered 1 through 9 from top to bottom, and the connectors are lettered A through F from left to right.

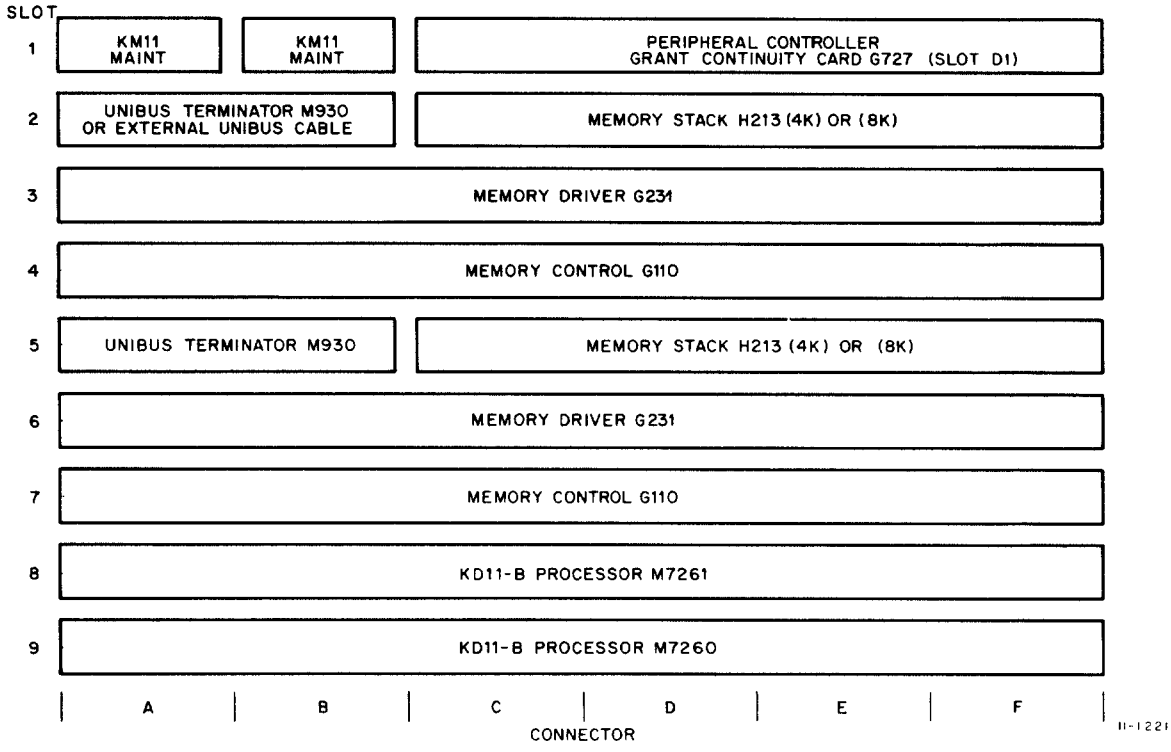

Figure 1-1 Module Utilization Diagram for Configuration 1 (16K)

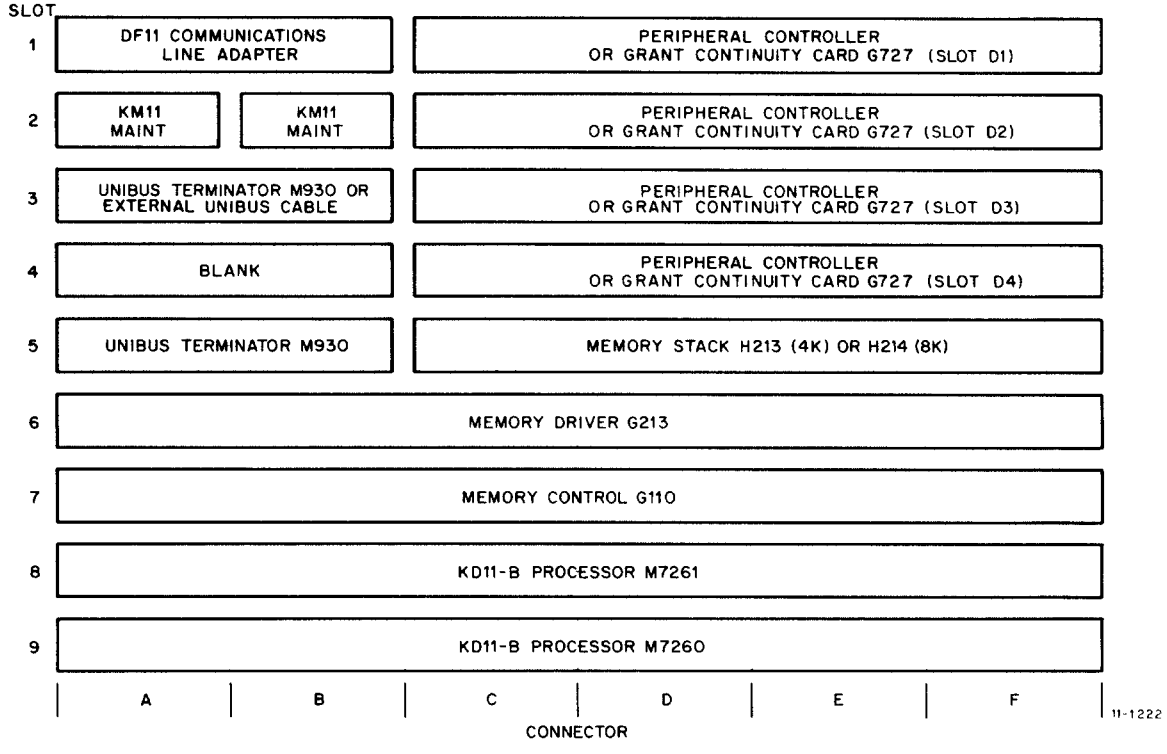

Figure 1-2 Module Utilization Diagram For Configuration 2 (8K)

Configuration 1 is the 16K version (Figure 1-1). Unibus M930 Terminator Modules are installed in slots A2-B2 and A5-B5. If other peripherals are to be connected to the computer, the terminator module in slot A2-B2 must be replaced with a BC11A Unibus cable, and a terminator module must be installed in the last device in the system. Slot C1-F1 provides the only space for a small peripheral controller. If this slot is not used, A G727 Grant Continuity Module must be installed in slot D1. If a small peripheral controller is to be installed, the G727 module must be removed first. Slots A1 and B1 are wired for the KM11 Maintenance Module. The core memories (3 modules each) are physically interchangeable as systems.

Configuration 2 is the 8K version (Figure 1-2). Unibus M930 Terminator Modules are installed in slots A3-B3 and A5-B5. If required, a BC11A Unibus cable can be installed in place of the terminator in slot A3-B3. Slots C1-F1, C2-F2, C3-F3, and C4-F4 can be used for small peripheral controllers. Slot A1-B1 is wired for a DF11 Communications Line Adapter that provides signal conditioning for communications devices using signals that are not TTL compatible. Slots A2 and B2 are wired for the KM11 Maintenance Module.

Figure 1-3 shows the backplane connector block configuration as viewed from the wirewrap pin side. The pin arrangement for each connector block is identical. It represents the total pins (36) available on the double-sided edge connector of a single height module. Connector A1 is shown in detail. Module contact designations are shown in Figure 1-4.

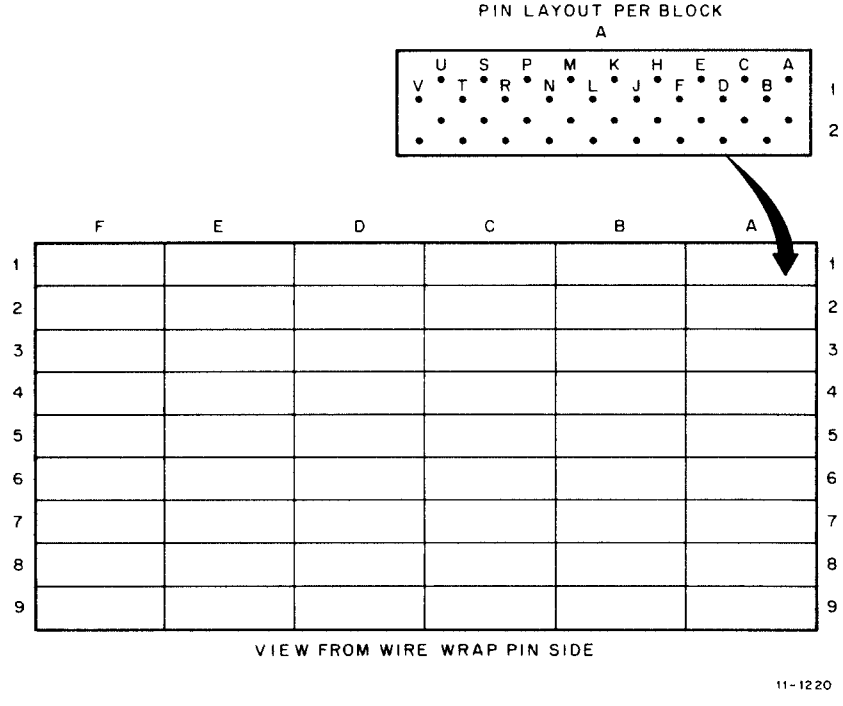

Figure 1-3 Computer Backplane Connector and Pin Designations

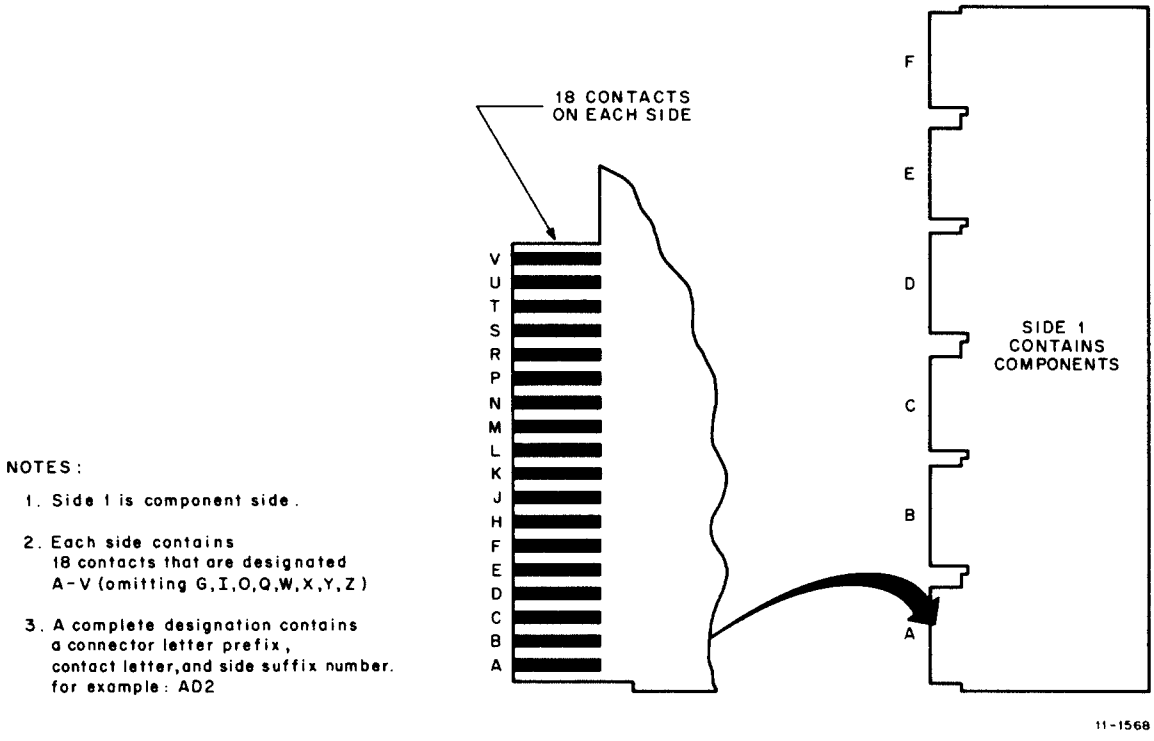

Figure 1-4 Module Contact Designations

1.3 ME11-L CORE MEMORY SYSTEM

Additional core memory is available for the computer in the self-contained add-on ME11-L Core Memory System. The basic ME11-L consists of an 8K MM11-L memory and power supply installed in a mounting box. It is expandable to 16K words or 24K words maximum by adding one or two more MM11-L memories. The ME11-L uses the same backplane construction as the computer. Nine slots are provided and they are wired to accommodate three MM11-L memories. These core memories (3 modules each) are physically interchangeable as systems and as individual modules within a system for troubleshooting purposes. If only one memory is used, the modules must be installed in the three bottom slots (7, 8, and 9).

1.4 EXTENSION MOUNTING BOX

Additional interface logic for the computer is installed in an extension mounting box identical to those used for the rest of the PDP-11 family. A rack-mounted box (BA11-ES) or a tabletop box (BA11-EC) can be used. The mounting box contains cooling fans, filter, and power cord. Space is provided to install six system units and an H720 Power Supply. Details of the extension mounting box, system units, and H720 Power Supply are included in the *PDP-11 Peripherals Handbook.*

CHAPTER 2
UNIBUS

2.1 INTRODUCTION

This chapter describes in general the operation of the Unibus.

The following documents, in conjunction with this manual, will aid the reader in understanding interface techniques and the overall PDP-11 system.

a. PDP-11/05, 11/10 Processor Handbook
b. PDP-11 Peripherals Handbook
c. Digital Logic Handbook

All communication between PDP-11 system components is through the high-speed Unibus. The Unibus operational concepts are vital to the understanding of the hardware and software implications of the Unibus.

2.2 UNIBUS STRUCTURE

The Unibus is a single common path that connects the processor, memory, and all peripherals. Addresses, data, and control information are transmitted along the 56 lines of the bus.

Every device on the Unibus employs the same form of communication; thus, the processor uses the same set of signals to communicate with memory and with peripheral devices. Peripheral devices also communicate with the processor, memory, or other peripheral devices via the same set of signals.

All instructions applied to data in memory can be applied equally well to data in peripheral device registers, enabling peripheral device registers to be manipulated by the processor with the same flexibility as memory. This feature is especially powerful, considering the capability of PDP-11 instructions to process data in any memory location as though it were an accumulator.

2.2.1 Bidirectional Lines

Most Unibus lines are bidirectional, allowing input lines to also be driven as output lines. This is significant in that a peripheral device register can be either read or used for transfer operations. Thus, the same register can be used for both input and output functions.

2.2.2 Master/Slave Relationship

Communication between two devices on the bus is based on a master/slave relationship. During any bus operation, one device, referred to as the bus master, has control of the bus when communicating with another device, the slave. A typical example of this relationship is the processor (master) transferring data to memory (slave). Master/slave relationships are dynamic. The processor, for example, passes bus control to a disk; the disk, as master, then communicates with a slave memory.

The Unibus is used by the processor and all I/O devices; thus, a priority structure determines which device gains control of the bus. Consequently, every device on the Unibus capable of becoming bus master has an assigned priority. When two devices capable of becoming bus master have identical priority values and simultaneously request use of the bus, the device that is electrically closest to the bus receives control.

2.2.3 Interlocked Communication

Communication on the Unibus is interlocked between devices. Each control signal issued by the master device must be acknowledged by a response from the slave to complete the transfer. Consequently, communication is independent of the physical bus length and the response time of the master and slave devices. The maximum transfer rate on the Unibus, with optimum device design, is one 16-bit word every 400 ns or 2.5 million 16-bit words per second.

2.3 PERIPHERAL DEVICE ORGANIZATION AND CONTROL

Peripheral device registers are assigned addresses similar to memory; thus, all PDP-11 instructions that address memory locations can become I/O instructions, enabling data registers in peripheral devices to take advantage of all the arithmetic power of the processor.

The PDP-11 controls devices differently than most computer systems. Control functions are assigned to a register address, and then the individual bits within that register can cause control operations to occur. For example, the command to make the paper-tape reader read a frame of tape is provided by setting a bit (the reader enable bit) in the control register of the device. Instructions such as MOV and BIS may be used for this purpose. Status conditions are also handled by the assignment of bits within this register, and the status is checked with TST, BIT, and CMP instructions.

2.4 UNIBUS CONTROL ARBITRATION

The Unibus is capable of performing two basic and parallel tasks in order to allow transfers by multiple peripherals at maximum speed. The first is the actual transfer of data between the current bus master and its addressed slave. The second is the selection of the next bus master, the peripheral which will be allowed to assert control as soon as the bus becomes free. It is important to note that the granting of future mastership is in no way influenced by either the current master or its method of obtaining the bus. It is this fact which allows these functions to be performed in parallel and allows transfers on the bus at a maximum rate.

2.4.1 Priority Transfer Requests

To gain mastership of the Unibus, a peripheral must first make a request to the processor for the bus and then wait for its selection. The processor contains the logic necessary to arbitrate these requests because normally there are several requests pending at any given time.

There are two classes of requests: bus requests and non-processor requests. A bus request (BR) is simply a request by a peripheral to obtain control of the Unibus with the understanding by the processor that the peripheral may end its use of the bus with a processor interrupt. An interrupt is a command to the processor to begin executing a new routine pointed to by a location selected by a device. A non-processor request (NPR) is similarily a request for the bus, but with the exception that it may not interrupt the processor. Since the granting of an NPR cannot affect the execution of the processor, it can occur during or between instructions. BRs however, by possibly causing execution to be diverted to a totally new routine, can only be granted between instructions. In this way, NPRs are assigned priority over any BR.

Between bus requests, there are four levels of priority created by four separate request lines. They are assigned priority levels 4 through 7; BR4 is the lowest and BR7 is the highest. These levels are associated with the program controlled priority level of the processor controlled by bits 7, 6, and 5 of the processor status register. Only BRs on a priority level higher than the level of the processor are eligible for receiving a bus grant. Thus, during high priority program tasks, all or selected Unibus requests (hence interrupts) can be inhibited by raising the level of the processor priority.

Another form of priority arbitration occurs through the system configuration. When the processor grants a request, the grant travels along the bus until it reaches the first requesting device which terminates the grant. Therefore, along the same grant line, the device electrically nearest the processor has the highest priority. Also note that in the KD11-B, the internal line clock is logically the last device on BR6, and the serial communication line interface is logically the last device on BR4.

After a requesting device receives a bus grant it asserts its selection as next bus master until the bus is free, thus inhibiting other requests from being granted. When the bus becomes free, the selected device asserts control of the bus and relinquishes its selection as next bus master so that the priority arbitration among pending requests may continue.

2.4.2 Processor Interrupts

After gaining control of the bus through a BR, a device can perform one or more transfers on the bus and/or request a processor interrupt. This is typically requested after a device has completed a given task; e.g., typing a character or completing a block data transfer through NPRs. If a peripheral wishes to interrupt the processor, it must assert the interrupt after gaining control of the bus but before relinquishing its selection as next bus master. Thus the processor knows that it may not fetch the next instruction, but must wait for the interrupt to be completed. Along with asserting the interrupt, the device asserts the unique memory address, known as the interrupt vector address, containing the starting address of the device service routine. Address vector +2 contains the new processor status word (PSW) to be used by the processor when beginning the service routine. After recognizing the interrupt, the processor reads the vector address and saves it in an internal register. It then pushes the current PSW and program counter onto the stack and loads the new program counter (PC) and PSW from the vector address specified. The service routine is then executed.

NOTE

These operations are performed automatically and no device polling is required to determine which routine to execute.

The device service routine can cause the processor to resume the interrupted process by executing the return from interrupt (RTI) instruction which pops the top two words from the processor stack and transfers them back to the PC and PS registers.

2.4.3 Data Transfers

After asserting control of the Unibus, the device does not release control until it has completed either one or more data transfers or an interrupt. Typically, only one transfer is completed each time the device gains control of the bus because few single devices can give or receive information at the maximum Unibus rate. Holding the bus for multiple transfers inhibits other devices from using the bus.

A transfer is initiated by the master device asserting a slave address and control signals on the bus and a master or address validity signal. The appropriate slave recognizes the valid address, reads or writes the data, and responds with a transfer complete signal. The master recognizes the transfer complete, sends or accepts data, and drops the address validating signal. It can then assert a new address and repeat the process or release control of the bus completely.

The importance of this type of structure is that it enables direct device-to-device transfers without any interaction from the central processor. An NPR device, such as a high speed CRT display, can gain fast access to the bus and transfer data at high rates while refreshing itself from memory without slowing down the processor.

CHAPTER 3
UNPACKING AND INSTALLATION

3.1 INTRODUCTION

The computer is shipped ready to operate in either a protective box or a 19-inch cabinet. Unless required by peripherals, there are no special shipping mounts internal to the computer. Prior to final electrical testing, each computer is thermal cycled, vibrated, and subjected to mechanical shock with all modules in place.

Basic computers are shipped in the package illustrated in Figure 3-1. Sufficient hardware is included in the shipping carton to rack mount the computer.

3.2 UNPACKING

Remove the computer from the box and remove the protective plastic cover from the console. Slide mounts are attached to the computer, but mounting screws are packed in a bag located in the same box. Also included is one 83600 Serial Communication Line (SCL) cable and two keys for the console lock. The 83600 SCL cable has a Berg 127009-0, 40-pin connector on one end that matches the SCL output connector on the computer. The other end of the 83600 SCL cable terminates in a Mate-N-Lok 1209340 which matches that used on the VT05, LA30, and Model 33 ASR Teletype®.

If the computer was ordered as a system with options requiring small peripheral controllers, the controllers may be inside the computer box. Small peripheral controllers are used to interface options such as a line printer or paper-tape reader/punch, as well as to implement a device such as a programmable clock.

After removing the computer from its package, it should be inspected for damage. It is advisable to save the packing carton in case it is necessary to return the unit for service.

A computer shipped in a 19-inch cabinet is locked in place by a metal lock attached to the rear of each slide assembly. Each lock is J-shaped and is attached by an 8-32 screw that passes through the slot in the chassis section of the slide and is threaded into the longer leg of the lock. The shorter leg is hooked around the end of the cabinet section of the slide to prevent extension of the slide. Both locks must be removed in order to slide the computer out of the cabinet. Retain the locks and screws for re-use if the equipment is to be shipped or moved any distance.

3.3 MECHANICAL DESCRIPTION

Figure 3-2 illustrates the 5-1/4 by 19 by 20 inch computer mounting box, including rack-mountable slide and console. The removable top cover of the mounting box is fastened by four Cam-Lock screws. The removable side panel is fastened by four Phillips-head screws.

Figure 3-3 shows the mounting box with the top cover removed. The backplane unit divides the power supply from the module side of the mounting box. The internal SCL cable runs from the backplane under the power supply unit to the rear of the mounting box.

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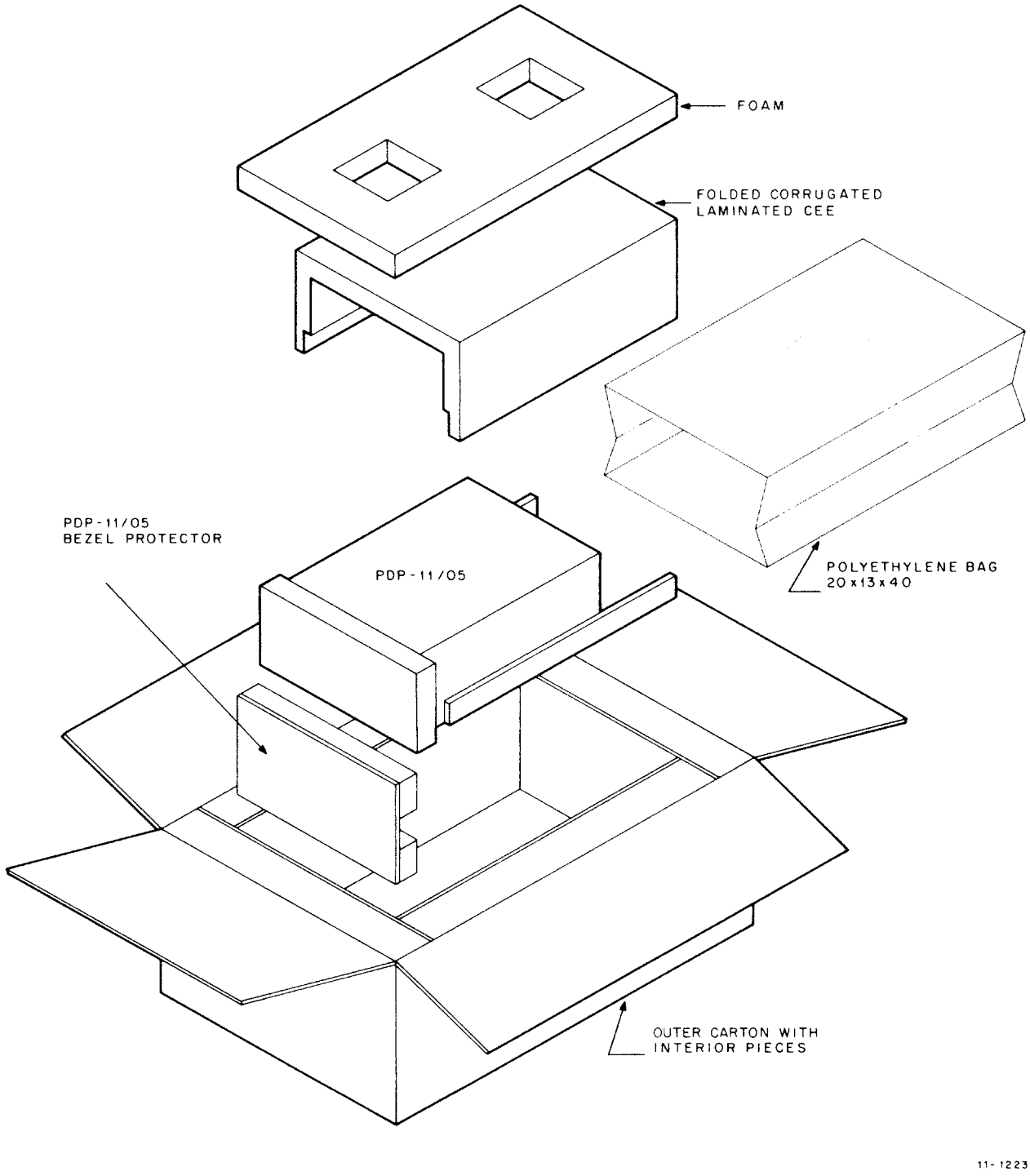


Figure 3-1 Computer Packaging

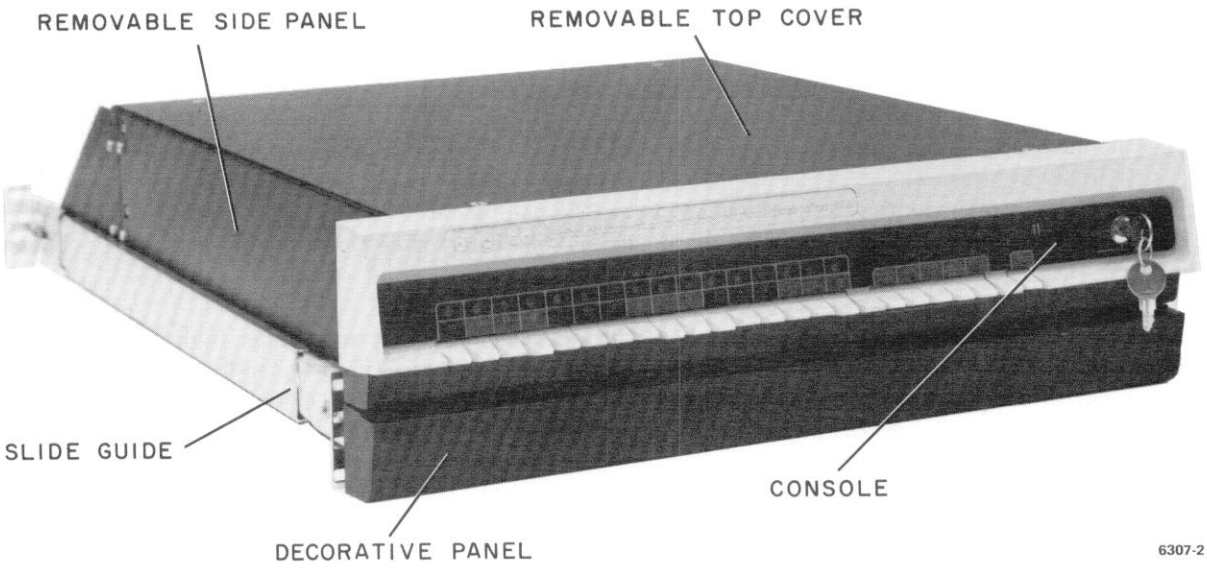


Figure 3-2 Computer Mounting Box

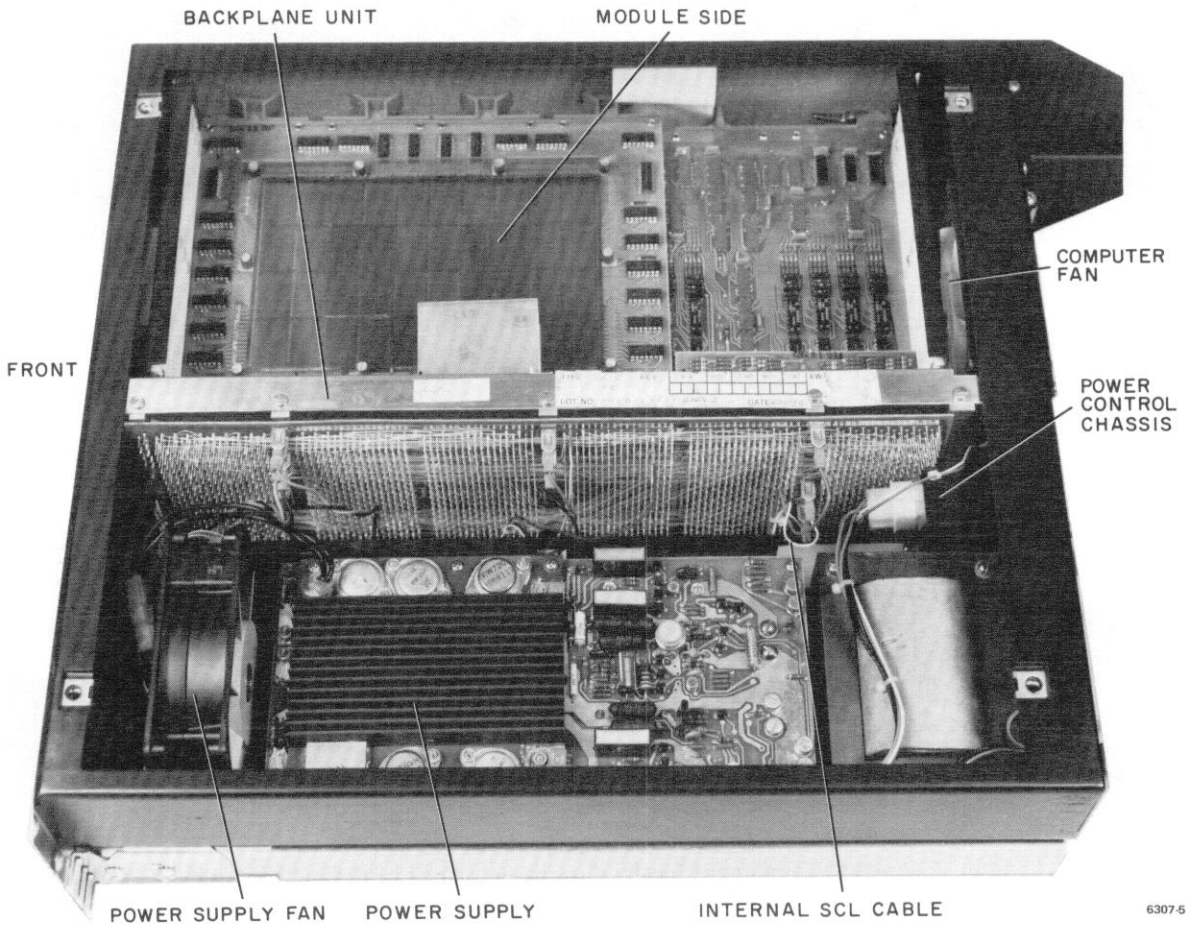


Figure 3-3 Computer Box With Top Cover Removed

Figure 3-4 shows the mounting box with top cover and side panel off, and the processor and memory modules plugged in. In this case, the computer is a Configuration 2 machine, using an MM11-L, 8K memory unit. Three small peripheral controllers are shown with the external cables attached. A G727 Grant Continuity Card is in the top peripheral slot and an M930 Unibus Terminator Card is in slot A3, B3. In Figure 3-5, the Unibus cable is in place, replacing the Unibus terminator card.

Figure 3-6 shows the mounting box without modules. The path of the console cable is under the M7260 Processor Module, then up and over to plug into the top of the M7260. The module guides aid in inserting the modules into proper slots.

Figure 3-7 is a rear view of the mounting box with attached rack-mountable slides. If the computer contains peripheral controllers outside the mounting box, the Unibus is extended from under the top cover. The power control circuit breaker protects the power supply from overload. It is rated at 7A for 110V units or 4A on 230V. The SCL connector and ac remote power control connectors are also shown.

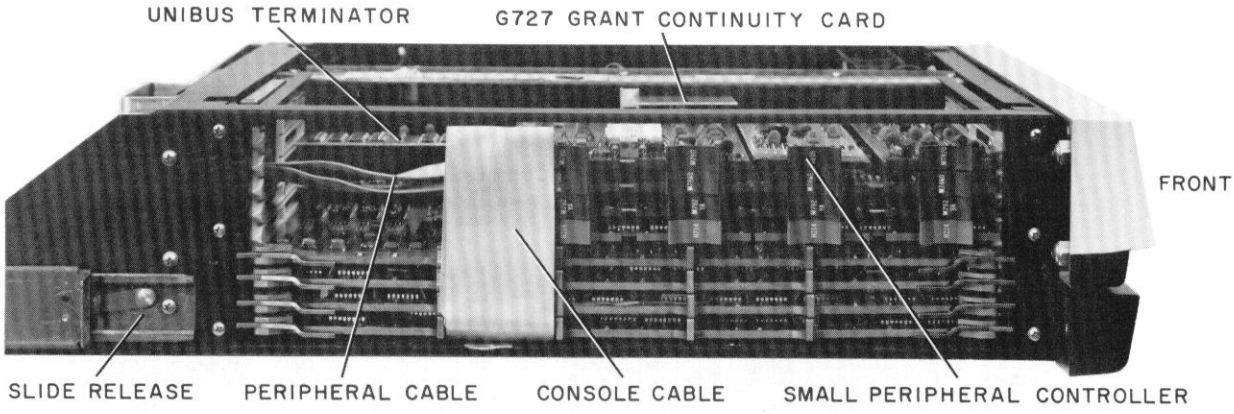


Figure 3-4 Computer Box with Top and Side Covers Removed

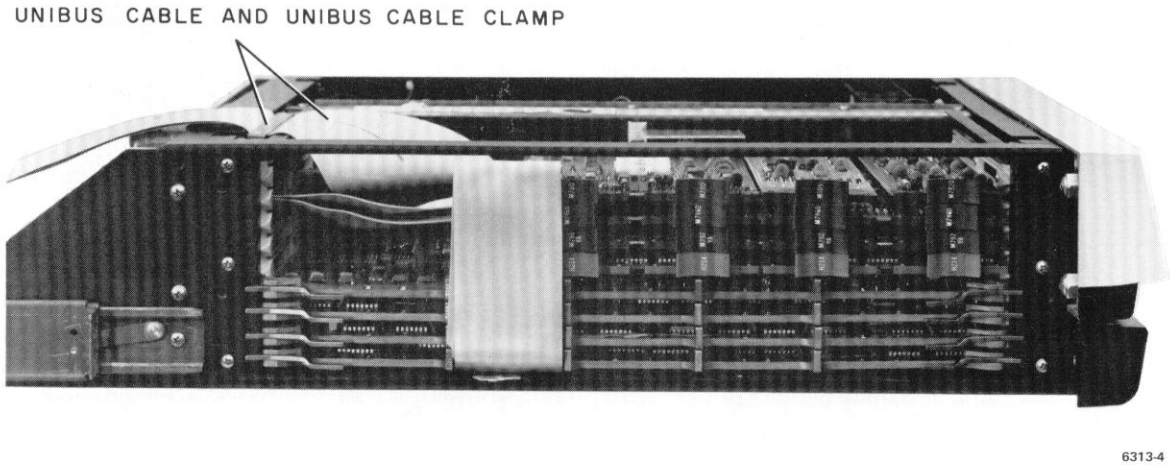


Figure 3-5 Computer Chassis (showing peripheral cables and the Unibus)

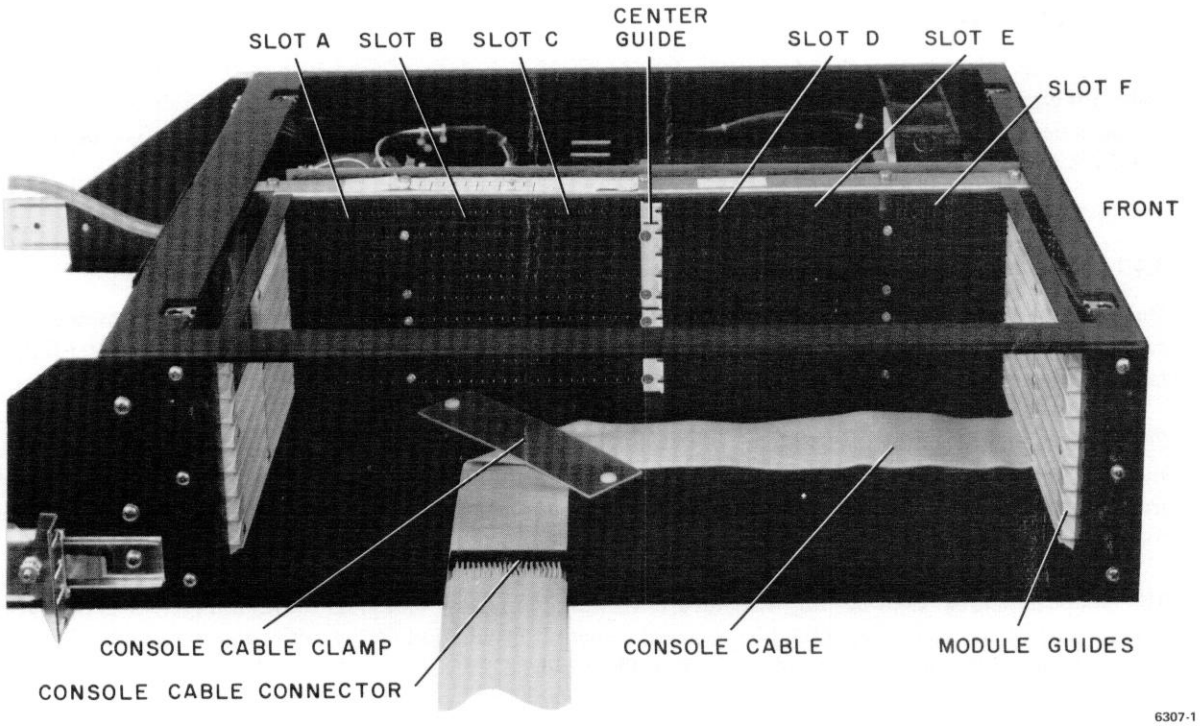


Figure 3-6 Mounting Box Without Modules

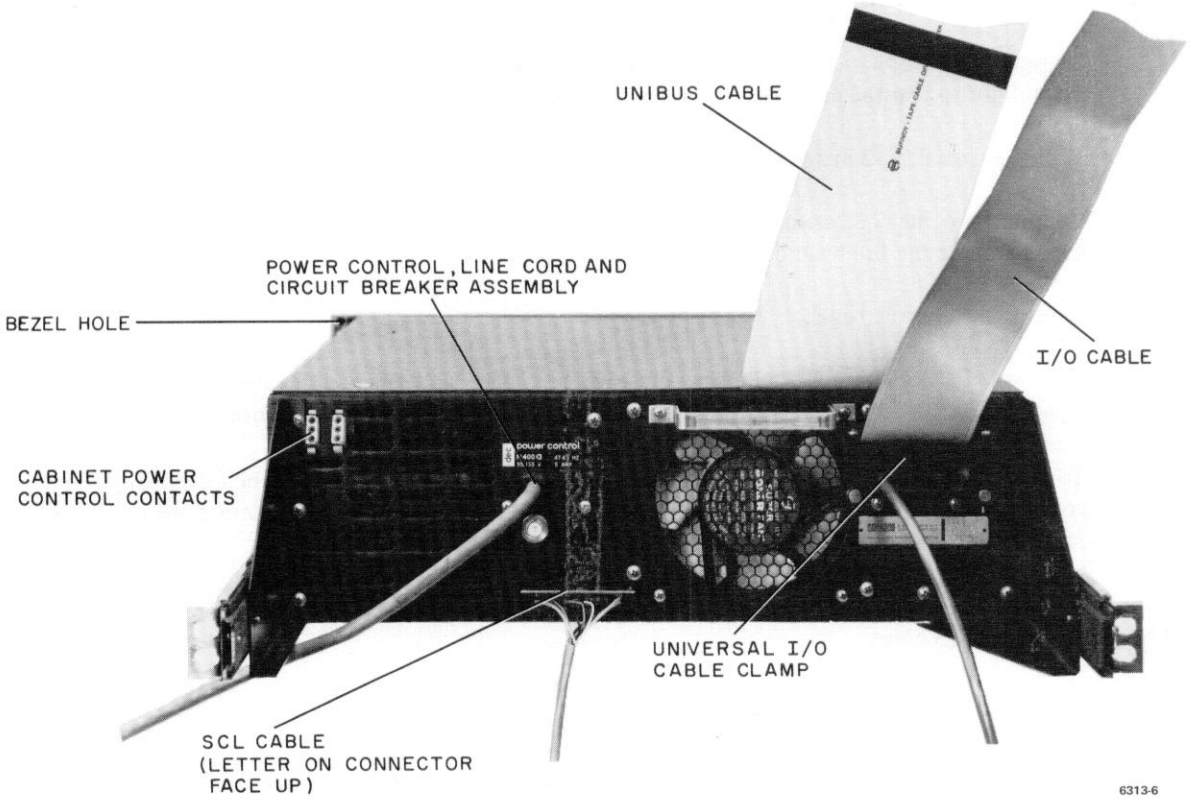


Figure 3-7 Rear of Computer With Cable Strain Reliefs

3.4 INSTALLATION

The computer mounts in a standard 19-inch wide by 25-inch deep equipment bay. The computer is mounted on slides for easy service. To mount the unit, first attach the fixed portion of the slides to the cabinet; the fixed portion of the slides can be removed from the computer by actuating the slide release shown in Figure 3-4. Be sure to mount the slides so that the fixed guides are parallel and level with the ground.

3.4.1 Mounting Computer on Installed Slides

Once the slide guides have been securely fastened in the cabinet using all eight screws, lift the computer and slide it carefully onto the slide guides until the slide release locks. Lift the slide release and push the computer fully into the rack, being careful not to tear any existing cabling.

Slightly loosen all eight cabinet slide mounting screws. Slide the computer back and forth several times to allow the slides to assume an optimum position. Push the computer into the cabinet as far as possible, leaving access to the front mounting screws. Tighten all eight cabinet slide mounting screws. Slide the computer back and forth and check for binding of the slides. If there is binding, repeat the above procedure until it is eliminated.

The computer should then be fully extended until the slide release locks. As shown in Figure 3-4, the panel on the module side of the computer should be removed to permit installation of I/O cables and the Unibus if required. The panel is removed by loosening and removing four Phillips-head screws.

3.4.2 Securing Computer to Cabinet Rack

If the rack-mounted computer is used in a moving environment, it must be secured to the cabinet rack to prevent the machine from moving on its slides. This option, if desired, is implemented as follows:

1. Remove the console bezel from the computer by removing the four screws at the rear of the bezel, being careful not to tear the cable that connects the console and processor.

2. Drill the partial 7/32-inch holes at each top inside corner of the bezel through from the rear of the bezel.

3. Counter-bore the 7/32-inch holes at the front of the console bezel 1/2 inch in diameter to a depth to accommodate the full head of a 10-32 machine screw.

4. Replace the console bezel.

5. Use two 10-32 by 2-inch Phillips-head screws and two Tinnerman nuts (PN 9007786) to secure the computer to the cabinet rack through the bezel holes at the desired rack position.

6. To make the 10-32 by 2-inch Phillips-head screws captive, machine a 1/8-inch deep by 1/8-inch wide groove, in each 10-32 by 2-inch Phillips-head screw just above the threads toward the head and insert a 1/8 I.D. O-ring in each groove.

3.4.3 Installation of I/O Cables

Flat and round I/O cables should be fed through the universal I/O cable clamp shown in Figure 3-6 for strain relief. They should then be connected to the appropriate small peripheral controllers. Note that the strain relief clamp prevents tension on the cables from damaging the connector block inside the computer. The wide Unibus cable, if required, should be folded as shown in Figure 3-5 and routed over and through a clamp attached to the top of the fan as shown in Figure 3-7. Note that there is a guide extending from the fan that prevents the Unibus cable from blocking air flow to the computer.

As shown in Figure 3-4, systems in which the Unibus is terminated in the computer box must have an M930 Terminator Card in slot A3-B3 as well as in slot A5-B5.

3.5 INTERCHANGEABLE PERIPHERAL SLOTS

The four peripheral slots in Configuration 2 are identical; therefore, it is possible to arrange the small peripheral controllers for the best mechanical convenience. For example, to diagnose a failure in a small peripheral controller, it may be convenient to place the selected option in the top slot where its components will be exposed.

3.6 SIDE AND TOP COVER INSTALLATION

Figures 3-4 and 3-5 show the computer ready for installation of the side cover. Note that the console cable is folded into a flat loop in order to clear the side cover. Attached to the side cover is the continuation of the left-hand slide. All four 8-32 screws that hold the cover in place should be inserted and tightened securely. The top cover can now be installed using the four Cam-Lock screws.

3.7 AC POWER SUPPLY CONNECTION

Computers designed for use on 115-Vac circuits are equipped with a 3-prong connector, which, when inserted into a properly wired 115-Vac outlet, grounds the case of the computer. It is unsafe to operate the computer unless the case is grounded since normal leakage current from the power supply flows into metal parts of the chassis.

If the integrity of the ground circuit is questionable, the user is advised to measure the potential between the computer case and a known ground with an ac voltmeter.

3.7.1 Connecting to Voltages Other than 115V

The computer will operate at voltages ranging from 95V to 135V and from 190V to 270V (47 Hz – 63 Hz), providing the proper power control is attached to the computer. The computer is ordered for nominal voltages of 115V or 230V. The standard 3-prong connector for 115V is identical to that found on most household appliances. A standard 3-prong connector is also used for 230V.

On installations outside of the United States or where the National Electrical Code does not govern building wiring, the user is advised to proceed with caution.

3.7.2 Quality of AC Power Source

Computer systems consisting of CPU, memory, and peripherals are often sensitive to the interference present on some ac power lines. If a computer system is to be installed in an electrically "noisy" environment, it may be necessary to condition the ac power line. DEC Field Service Engineers can assist customers in determining if their ac line is satisfactory.

3.8 CABINET POWER CONTROL

Provisions have been made for the computer switch to operate a cabinet power control. This feature permits the computer key lock switch to control the power supply for peripherals attached to the computer (Part 4). The power control contacts are closed when the key lock switch is in the POWER or PANEL LOCK positions. The wiring diagram for a typical cabinet power control system is shown in Figure 3-8. The power control contacts of the computer may be used to switch a maximum of 230V at 4A.

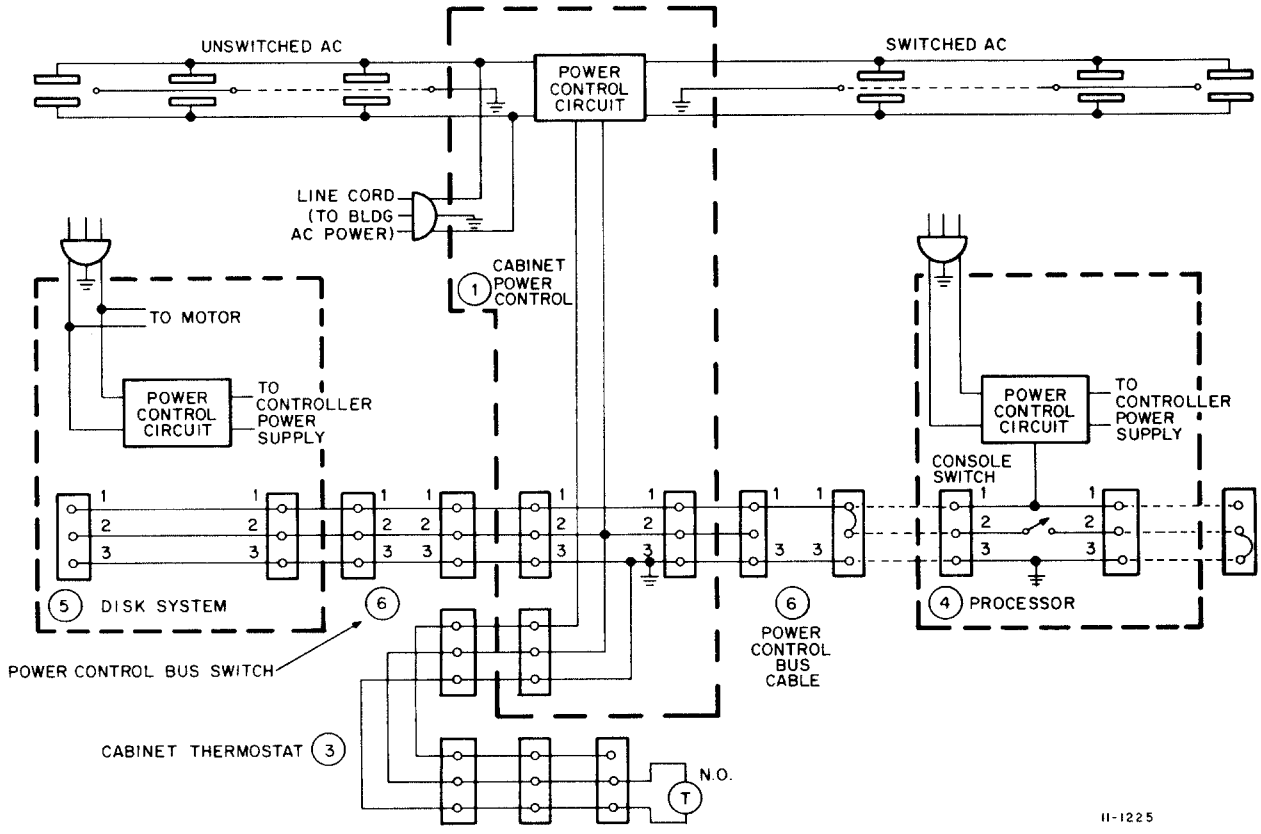


Figure 3-8 Typical Cabinet Power Control System Wiring Diagram

3.9 INSTALLATION CERTIFICATION

Once the computer has been installed, it is strongly recommended that a system diagnostic be run to ensure that the equipment operates correctly and that installation has been properly performed. Because system configurations widely vary, no one diagnostic will completely exercise all the attached devices.

The *MAINDEC User's Manual* that comes with the diagnostic package should be consulted for the appropriate diagnostic to be run, depending upon the attached devices. The *MAINDEC User's Manual* lists the devices that each diagnostic will exercise. The three system exercisers presently available are T17 System Exerciser (MAINDEC-11-DZKAP) for relatively small systems, General Test Program (MAINDEC-11-DZQGA) for medium to large systems, and Communications Test Program (MAINDEC-11-DZQCA) for communications-oriented systems. At least one of the above diagnostics and, if appropriate, the other two, should be used to verify system operation.

Once the diagnostic is selected, the respective diagnostic write-up should be consulted for specific operating instructions. If the user is not familiar with console operation and/or procedures for loading paper tapes, he should read Chapter 4 of this manual.

3.10 WARRANTY SERVICE (Domestic Only)

If the machine is still covered under the 30 day return-to-factory warranty, and it is desired to return it for factory service, the following procedure should be used. If the machine is no longer on warranty, the local DEC Field Service office should be contacted.

1. Call the Maynard, Massachusetts Repair Depot, Telephone 617-897-5111, X4079 or X2135.

2. The caller will receive an RA (Return Authorization) number, which must appear on the shipping label of the package being returned.

3. Package the machine in an equivalent shipping container, similar to the one the computer arrived in. If possible, use the original computer shipping container.

4. Send the machine to the following address:

   Digital Equipment Corporation
   146 Main Street
   Maynard, Massachusetts 01754
   Att: Depot Repair, Bldg, 21-4

   RA # XXXX

CHAPTER 4
COMPUTER OPERATION

4.1 INTRODUCTION

This chapter assumes that the computer is installed and connected to the ac power line. It is also assumed that the reader has access to the appropriate diagnostic materials, and a copy of the absolute loader paper tape. It is further assumed that the user is using paper tapes to load software and diagnostics. For systems that have mass storage services, i.e., disks or DECtape, the user should refer to the appropriate software manuals for mass storage operating systems.

4.2 POWER SWITCH OPERATION

The key lock power switch shown in Figure 4-1 has three positions:

OFF – Fully counterclockwise
POWER – 90° clockwise from OFF
PANEL LOCK – 180° clockwise from OFF

In the OFF position, ac power is removed from the primary of the computer power supply, and the cabinet power control contacts are open-circuited. In the other two positions, the ac power is applied to the computer power supply and the cabinet power control contacts are short-circuited. In the POWER position, the console function switches (the right six switches in Figure 4-1) are fully operative. In the PANEL LOCK position, the console function switches have no effect on the computer's operation. PANEL LOCK is used to secure a running computer from mischievous tampering.

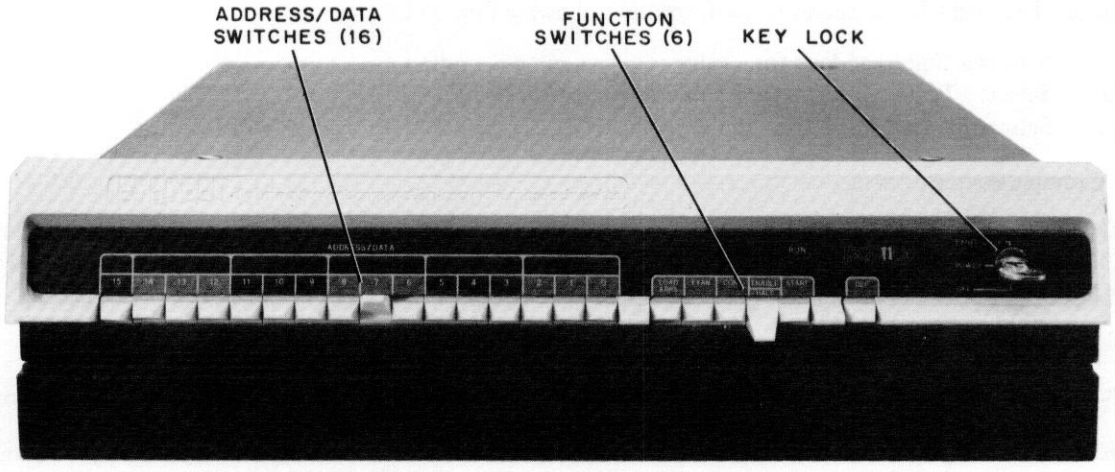


Figure 4-1 Console Illustrating Switch Movements

4.3 FUNCTION SWITCHES

The right six switches in Figure 4-1 are called function switches. They are listed below in order of their appearance from left to right.

1. LOAD ADRS (load address)
2. EXAM (examine)
3. CONT (continue)
4. ENABLE/HALT
5. START
6. DEP (deposit)

Function switches 1 through 5 are actuated by being depressed as is the ENABLE/HALT switch in Figure 4-1. The DEP switch must be lifted for actuation. All of the function switches, with the exception of ENABLE/HALT, are spring loaded and return to their rest state when released.

4.4 ADDRESS/DATA SWITCHES

The 16 ADDRESS/DATA switches are to the left of the function switches (Figure 4-1). These 2-position switches represent a manually set flip-flop register with the up position representing a logical 1 and the down position a logical 0. The ADDRESS/DATA switches may be used in conjunction with the function switches or in conjunction with a program stored in the computer's memory. The ADDRESS/DATA switches are often referred to as the Switch Register in DEC documentation. In Figure 4-1, the contents of the Switch Register is equal to 200_8 because bit 7 is set to a 1 and all others are set to a 0.

4.5 CONSOLE INDICATORS

There are 17 indicators on the computer console. The contents of the 16 ADDRESS/DATA lights either represent a 16-bit Unibus address or the contents of a 16-bit Unibus address. Note that the state of the ADDRESS/DATA lights is defined only when the computer RUN light is not illuminated.

4.6 CONSOLE OPERATION

The following paragraphs describe the operation of the function switches. Table 4-1 indicates the meaning of the ADDRESS/DATA lights for all cases where the contents of these lights are defined.

4.6.1 Load Address Switch

Depressing the LOAD ADRS switch when the computer is halted causes the contents of the Switch Register to be stored in a temporary register within the computer. This data is also displayed in the ADDRESS/DATA lights for verification. The load address operation performs the following functions:

a. Selects a Unibus address for a subsequent examine operation.
b. Selects a Unibus Address for a subsequent deposit operation.
c. Selects the starting address of a program.

4.6.2 Examine Switch

The EXAM switch permits the display of the contents of a selected Unibus address in the ADDRESS/DATA lights. Select the appropriate address in the Switch Register and depress the LOAD ADRS switch. Then depress and release the EXAM switch. The contents of the selected address will then be displayed in the ADDRESS/DATA lights.

Several features are built into the examine function to aid in programming the computer.

a. While the EXAM switch is depressed, the address to be examined is displayed. The data itself is displayed when the switch is released.
b. If the EXAM switch is repeatedly depressed, the Unibus address is incremented by two on each depression*. This permits the examination of a list of addresses without repeated load address operations.

*The Unibus address is incremented by one when examining general registers.

Table 4-1
Significance of ADDRESS/DATA Indicators

Action	Qualification	Information Displayed In ADDRESS/DATA Indicators
Power On	1. ENABLE/HALT switch in HALT position	1. Contents of location $(24)_8$
	2. ENABLE/HALT switch in ENABLE position	2. Undefined – depends on contents of memory
Load Address	LOAD ADRS switch depressed	Contents of Switch Register
Examine	1. EXAM switch depressed	1. Unibus address that is to be examined
	2. EXAM switch released	2. Contents of Unibus address that was examined
Deposit	1. DEP switch raised	1. Unibus address that is to be deposited
	2. DEP switch released	2. Contents of Switch Register which is the data deposited
RUN Light On		Undefined
Program Halt	1. ENABLE/HALT switch in HALT position	1. Address of instruction to be executed when CONT switch is actuated
	2. HALT instruction executed	2. Same as 1
	3. Double bus error which is two successive attempts to access non-existent memory or improper odd byte address.	3. Contents of program counter (R7) at time double bus error occurred
Program Execution	1. START switch depressed	1. Address of last load address
	2. CONT switch depressed	2. Address of instruction to be executed

c. If an attempt is made to examine non-existent memory, it is necessary to perform the initialize operation explained in Paragraph 4.7.

d. Only full words are displayed in the ADDRESS/DATA lights; thus, bit 0, the byte address bit, is ignored when using the EXAM switch with the following exception. Note that the general registers are located on byte addresses. Therefore, when examining the general registers, address bit 0 is recognized and the increment feature is modified such that sequential registers may be examined by repeated use of the EXAM switch.

Note that the EXAM switch has no effect while the computer is in the RUN state or when the key operated power switch is in the PANEL LOCK position.

4.6.3 Deposit Switch

The physical operation of the DEP switch requires that it be lifted for actuation. The DEP switch permits the contents of the Switch Register to be deposited in a Unibus address, which is typically specified by a previous load address operation. To deposit the instruction BRANCH SELF (777_8) in location 200_8, first set the Switch Register to 200_8 as shown in Figure 4-1 and actuate the LOAD ADRS switch. Set the Switch Register to 777_8 then lift and release the DEP switch.

Several additional features are built into the deposit function:

a. While the DEP switch is actuated, the Unibus address to be effected is displayed in the ADDRESS/DATA lights. When the switch is released, the data deposited is displayed for verification.

b. If the DEP switch is repeatedly depressed, the Unibus address is incremented by two on each depression*. This permits the depositing of an entire program with only one load address operation.

c. If an attempt is made to deposit into non-existent memory, it is necessary to perform the initialize operation explained in Paragraph 4.1.

d. All deposit operations affect full 16-bit words. Bit 0 of the address is used only when depositing into general registers, otherwise, bit 0 of the address is ignored.

4.6.4 ENABLE/HALT Switch

Place the ENABLE/HALT switch in the HALT position (Figure 4-1); the computer will halt at the end of the current instruction, providing the key switch is not in the PANEL LOCK position. All interrupts and traps will be executed prior to halting. This switch may be used in conjunction with the CONT switch to step through programs (Paragraph 4.6.6). With the ENABLE/HALT switch in the ENABLE position, programs may be executed once started by: actuating the START switch, actuating the CONT switch, and the auto-restart power-up sequence.

4.6.5 START Switch

The sequence for starting a program from the console is as follows:

1. Set the starting address of the program in the Switch Register.
2. Depress the LOAD ADRS switch.
3. Position the ENABLE/HALT switch in the ENABLE position.
4. Depress and release the START switch.

While the START switch is depressed, the following actions occur:

1. An initialize signal is generated on the Unibus. This initialize signal serves to reset all peripherals.

2. The program status word is reset to zero.

3. The program counter, R7, is loaded with the last address loaded with the LOAD ADRS switch.

When the START switch is released, program execution begins with the instruction contained in the location specified by R7 and the RUN light is turned on. If the ENABLE/HALT switch is in the HALT position, the computer remains in the HALT state following the release of the START switch.

*The Unibus address is incremented by one when depositing into general registers.

Observe the following precautions when using the START switch:

a. If the keylock is not in the PANEL LOCK position, depressing the START switch while a program is running initializes the computer system and restarts the program.

b. It is good practice to precede every program start with a load address operation.

c. A program should not be started at an odd address or the first fetch operation will be aborted and an odd address trap will be attempted. If the stack pointer, R6, is not properly set up, the program in memory may be destroyed.

4.6.6 Continue Switch

The CONT switch is used to continue a program without altering the program counter, R7, or the machine state. To continue a halted program, depress and release the CONT switch. The program is resumed when the CONT switch is released.

The CONT switch is used with the ENABLE/HALT switch to step through programs one instruction at a time. If the CONT switch is actuated while the ENABLE/HALT switch is in the HALT position (Figure 4-1), a single instruction will be executed. Note that interrupts are serviced in single instruction mode. In single step mode, the address of the next instruction to be executed is displayed in the lights.

4.7 UNCONDITIONAL COMPUTER AND UNIBUS INITIALIZATION

Unconditional initialization of the computer system usually occurs because of an attempt to examine from, or deposit into, non-existent memory from the console. However, a peripheral or processor error may occur that can only be overcome by initializing the system from the console. The procedure is simply to depress the START switch with the ENABLE/HALT switch in the HALT position.

4.8 LOADING PROGRAMS FROM PAPER TAPE

When the computer is first received, the content of its memory is not defined (it knows absolutely nothing, not even how to receive paper-tape input). However, the computer can accept data when toggled directly into core using the console switches. The Bootstrap Loader program is the first program to be loaded, and therefore must be toggled into core. The loaders described in this section facilitate the loading of programs from either the low or high speed paper-tape reader. The low speed reader is part of the Model 33 ASR Teletype and is operated via the SCL. The high speed reader is DEC part number PC-11.

The Bootstrap Loader program instructs the computer to accept and store in core data that is punched on paper tape in bootstrap format. The Bootstrap Loader is used to load very short paper-tape programs of 162_8 16-bit words or less (primarily the Absolute Loader and Memory Dump programs). Programs longer than 162_8 16-bit words must be assembled into absolute binary format using the PAL-11A Assembler and loaded into memory using the Absolute Loader.

The Absolute Loader (Paragraph 4.8.2) is a system program that enables data punched on paper-tape in absolute binary format to be loaded into any available memory bank. It is used primarily to load the paper-tape system software (excluding certain subprograms) and object programs assembled with PAL-11A.

The loader programs are loaded into the upper most area of available memory so that they will be available for use with system and user programs. When writing programs, the locations used by the loaders should not be used without restoring their contents; otherwise, the loaders will have to be reloaded because the object program will have altered them.

Memory Dump programs are used to print or punch the contents of specified areas of memory. For example, when developing or debugging user programs, it is often necessary to get a copy of the program or portions of memory.

There are two dump programs supplied in the paper-tape software system: DUMPIT, which prints or punches the octal representation of all or specified portions of memory; and DUMPAB, which punches all or specified portion of memory in absolute binary format suitable for loading with the Absolute Loader.

4.8.1 The Bootstrap Loader

The Bootstrap Loader should be loaded (toggled) into the highest memory bank. The locations and corresponding instructions of the Bootstrap Loader are listed in Table 4-2 and explained below.

Table 4-2
Bootstrap Loader Instructions

Location	Instruction
XX7744	016701
XX7746	000026
XX7750	012702
XX7752	000352
XX7754	005211
XX7756	105711
XX7760	100376
XX7762	116162
XX7764	000002
XX7766	XX7400
XX7770	005267
XX7772	177756
XX7774	000765
XX7776	YYYYY

In Table 4-2, XX represents the highest available memory bank. For example, the first location of the loader would be as indicated in Table 4-3, depending on memory size, and XX in all subsequent locations would be the same as the first.

Note in Table 4-3 that the contents of location XX7766 should reflect the appropriate memory bank in the same manner as the preceding locations.

Table 4-3
Memory Bank Assignments

Location	Memory Bank	Memory Size
017744	0	4K
037744	1	8K
057744	2	12K
077744	3	16K
117744	4	20K
137744	5	24K
157744	6	28K

The contents of location XX7776 (YYYYYY in the instruction column of Table 4-2) should contain the device status register address of the paper-tape reader to be used when loading the bootstrap formatted tapes. Either paper-tape reader may be used, and the associated address is specified as follows:

Teletype Paper-Tape Reader – 177560
High Speed Paper-Tape Reader – 177550

4.8.1.1 Loading the Loader Into Memory – With the computer initialized for use as described in Paragraph 4.7, toggle in the Bootstrap Loader as explained below.

1. Set XX7744 in the Switch Register (SR) and press LOAD ADRS switch (XX7744 will be displayed).

2. Set the first instruction, 016701, in the SR and lift DEP switch (016701 will be displayed).

NOTE
When depositing data into consecutive words, the DEP switch automatically increments the address to the next word.

3. Set the next instruction, 000026, in the SR and lift DEP switch. Continue to deposit subsequent instructions.

4. Deposit the desired device status register address in location XX7776, the last location of the Bootstrap Loader.

NOTE
It is a good programming practice to verify that all instructions are stored correctly. Proceed to Step 6.

6. Set XX7744 in the SR and press LOAD ADRS switch.

7. Press and release EXAM switch (the octal instruction in location XX7744 will be displayed so that it can be compared to the correct instruction, 016701). If the instruction is correct, proceed to Step 8, otherwise go to Step 10.

8. Press EXAM switch. The instruction of the location displayed in the ADDRESS/DATA indicators with the switch depressed will be displayed when the switch is released. Compare the indicator contents to the instruction at the proper location.

9. Repeat Step 8 until all instructions have been verified or go to Step 10 if the correct instruction is not displayed.

NOTE
Whenever an incorrect instruction is displayed, it can be corrected by performing Steps 10 and 11.

10. With the incorrect instruction displayed in the ADDRESS/DATA register, set the correct instruction in the SR and lift DEP switch. The contents of the SR will be deposited in the location displayed with the key lifted.

11. Press EXAM switch to ensure that the instruction was correctly stored.

The Bootstrap Loader is now in core. The procedures above are illustrated in the flow chart of Figure 4-2.

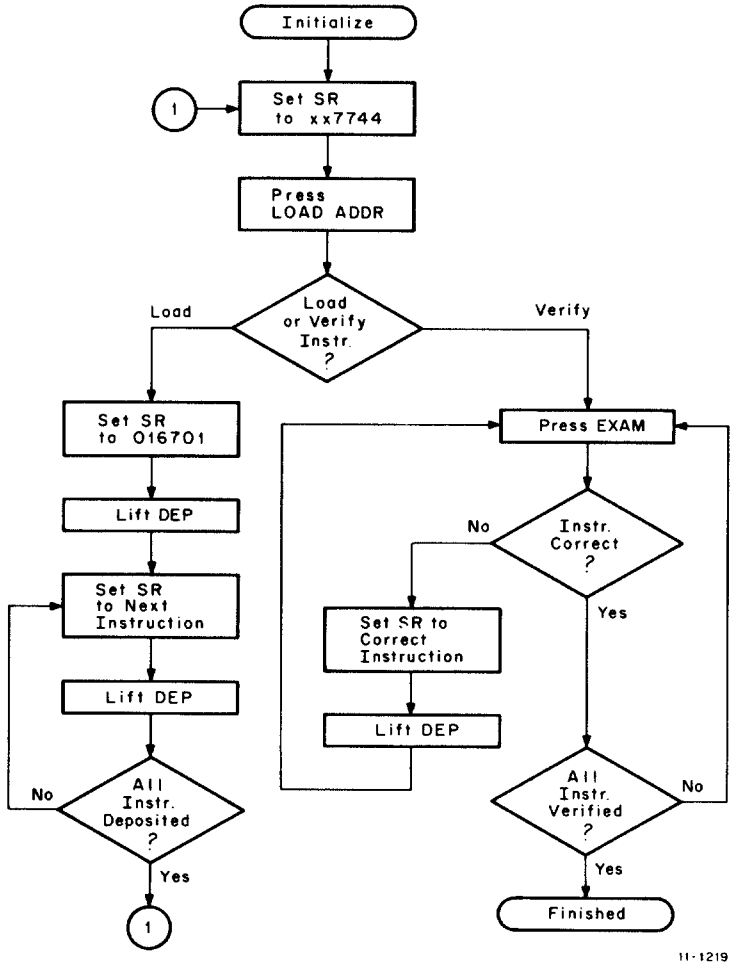


Figure 4-2 Loading and Verifying the Bootstrap Loader

4.8.1.2 Loading Bootstrap Tapes – Any paper tape punched in bootstrap format is referred to as a bootstrap tape and is loaded into memory using the Bootstrap Loader. Bootstrap tapes begin with about two feet of special bootstrap leader code (ASCII code 351, not blank leader tape as is required by the Absolute Loader).

With the Bootstrap Loader in memory, it will load the bootstrap tape into memory starting anywhere between location XX7400 and location XX7743; i.e., 162_8 words. The paper-tape input device used is specified in location XX7776. Bootstrap tapes are loaded into memory as explained below:

1. Set the ENABLE/HALT switch to HALT.

2. Place the bootstrap tape in the specified reader with the special bootstrap leader code over the reader sensors (under the reader station).

3. Set the SR to XX7744 (the starting address of the Bootstrap Loader) and press LOAD ADRS switch.

4. Set the ENABLE/HALT switch to ENABLE.

5. Press START switch. The bootstrap tape will pass through the reader as data is being loaded into memory.

6. The bootstrap tape stops after the last frame of data (Figure 4-5) has been read into memory. The program on the bootstrap is now in memory.

The procedures above are illustrated in the flowchart of Figure 4-3.

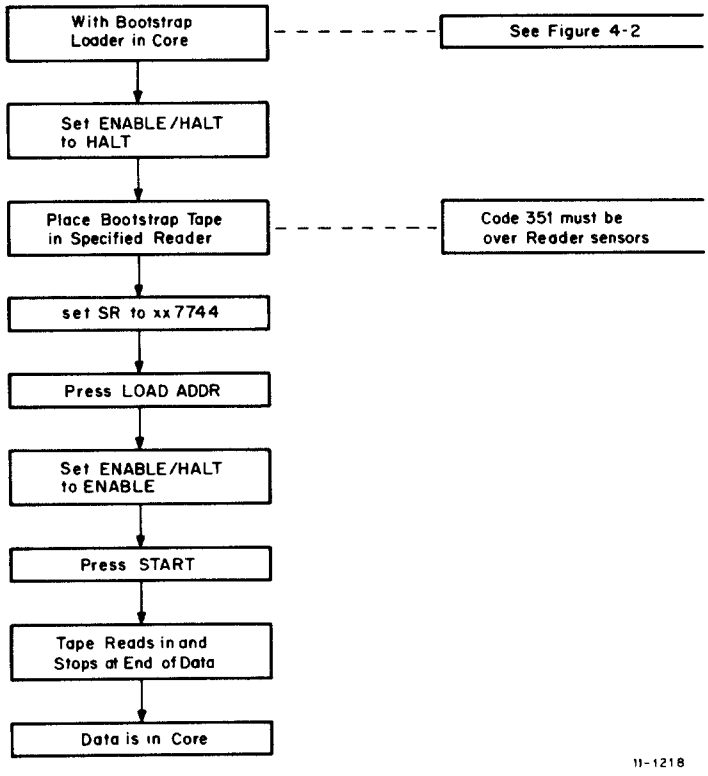


Figure 4-3 Loading Bootstrap Tapes Into Memory

If the bootstrap tape does not read in immediately after depressing the START switch, it is due to one of the following reasons:

a. Bootstrap Loader not correctly loaded
b. Using the wrong input device
c. Code 351 not directly over the reader sensors
d. Bootstrap tape not properly positioned in reader

4.8.1.3 Bootstrap Loader Operation – The Bootstrap Loader source program is shown below. The starting address in the example denotes that the program is to be loaded into memory bank zero (a 4K system).

The Bootstrap Loader source program is a brief but fairly complex example of the PAL-11A Assembly Language. Explanations of the program and PAL-11A are found in the *PDP-11 Paper-Tape Software Programming Handbook,* DEC-11-GGPB-D.

```
                000001              R1=%1           ;USED FOR THE DEVICE
                                                    ;ADDRESS
                000002              R2 %2           ;USED FOR THE LOAD AD-
                                                    ;DRESS DISPLACEMENT
                017400              LOAD=17400      ;DATA MAY BE LOADED NO
                                                    ;LOWER THAN THIS
                017744              .-17744         ;START ADDRESS OF THE
                                                    ;BOOTSTRAP LOADER
017744          016701    START:    MOV DEVICE, R1  ;PICK UP DEVICE ADDRESS,
                000026                              ;PLACE IN R1
017750          012702    LOOP:     MOV # .-LOAD+2, R2  ;PICK UP ADDRESS
                000352                              ;DISPLACEMENT
017754          005211    ENABLE:   INC @ R1        ;ENABLE THE PAPER TAPE
017756          105711    WAIT:     TSTD @ R1       ;READER
                                                    ;WAIT UNTIL FRAME
017760          100376              BPL WAIT        ;IS AVAILABLE
017762          116162              MOVB 2(R1), LOAD (R2)  ;STORE FRAME READ
                000002                              ;FROM TAPE IN MEMORY
                017400
017770          005267              INC LOOP+2      ;INCREMENT LOAD ADDRESS
                177756                              ;DISPLACEMENT
017774          000765    BRNCH:    BR LOOP         ;GO BACK AND READ MORE
                                                    ;DATA
017776          000000    DEVICE:   0               ;ADDRESS OF INPUT DEVICE
```

4.8.2 The Absolute Loader

The Absolute Loader is a system program that enables data punched on paper tape in absolute binary format to be loaded into any memory bank. It is used primarily to load the paper-tape system software (excluding certain subprograms) and object programs assembled with PAL-11A. The major features of the Absolute Loader include:

a. Testing of the checksum on the input tape to ensure complete, accurate loads

b. Starting the loaded program upon completion of loading without additional user action, as specified by the .END in the program just loaded

c. Specifying the load address of position independent programs at load time rather than at assembly time, by using the desired loader Switch Register option.

4.8.2.1 Loading the Loader Into Memory – The Absolute Loader is supplied on punched paper-tape in bootstrap format, therefore, the Bootstrap Loader is used to load the Absolute Loader into memory. It occupies locations XX7474 through XX7743, and its starting address is XX7500. The Absolute Loader program is 72_{10} words long, and is loaded adjacent to the Bootstrap Loader.

4.8.2.2 Loading Absolute Tapes – Any paper-tape punched in absolute format is referred to as an absolute tape, and is loaded into memory using the Absolute Loader. When using the Absolute Loader, there are two methods of loading available: normal and relocated.

A normal load occurs when the data is loaded and placed in memory according to the load addresses on the object tape. It is specified by setting bit 0 of the Switch Register to 0 immediately before starting the load.

There are two types of relocated loads:

a. Loading to continue from where the loader left off after the previous load. This type is used, when the object program being loaded is contained on more than one tape. It is specified by setting the Switch Register to 000001 immediately before starting the load.

b. Loading into a specific area of memory. This is normally used when loading position independent programs. A position independent program is one that can be loaded and run anywhere in available memory. The program is written using the position independent instruction format. The type of load is specified by setting the Switch Register to the load address and adding 1 to it (i.e., setting bit 0 to 1).

Optional Switch Register settings for the three types of loads are listed below.

	Switch Register	
Type of Load	**Bits 1-14**	**Bit 0**
Normal	(ignored)	0
Relocated - continue loading where left off	0	1
Relocated - load in specified area of memory	nnnnn (specified address)	1

The absolute tape may be loaded using either paper-tape reader. The desired reader is specified in the last word of available memory (XX7776). The input device status word may be changed at any time prior to loading the absolute tape. With the Absolute Loader in memory, absolute tapes are loaded as explained below:

1. Set the ENABLE/HALT switch to HALT. To use an input device other than that used for loading the Absolute Loader, change the address of the device status word (in location XX7776) to reflect the desired device; i.e., 177560 for the Teletype reader or 177550 for the high-speed reader.

2. Set the SR to XX7500 and press LOAD ADRS switch.

3. Set the SR to reflect the desired type of load.

4. Place the absolute tape in the proper reader with blank leader tape directly over the reader sensors.

5. Set ENABLE/HALT switch to ENABLE.

6. Press START switch. The absolute tape will begin passing through the reader station as data is being loaded into memory.

If the absolute tape does not begin passing through the reader station, the Absolute Loader is not in memory correctly. Reload the loader and start over at Step 1. If it halts in the middle of the tape, a checksum error occurred in the last block of data read in.

Normally, the absolute tape will stop passing through the reader station when it encounters the transfer address as generated by the statement .END, denoting the end of a program. If the system halts after loading, check that the low byte of R0 is 0*. If so, the tape is correctly loaded. If not 0, a checksum error has occurred in the block of data just loaded, indicating that some data was incorrectly loaded. The tape should be reloaded starting at Step 1.

*To read R0, load address 177700 and press EXAM switch.

4.8.3 Memory Dumps

A Memory Dump program is a system program that enables the contents of all or any specified portion of memory to be dumped (print or punch) onto the teletype printer and/or punch, line printer, or high speed punch. There are two dump programs available in the paper-tape software system:

a. DUMPIT, which dumps the octal representation of the contents of specified portions of memory onto the teleprinter, low speed punch, high speed punch, or line printer.

b. DUMPAB, which dumps the absolute binary code of the contents of specified portions of memory onto the low speed or high speed punch.

Both dump programs are supplied on punched paper tape in bootstrap and absolute binary formats. Paragraph 4.8.1.3 explains how the Absolute Loader is loaded over the bootstrap tapes. The absolute binary tapes are position independent and may be loaded and run anywhere in memory as explained in Paragraph 4.8.2.2. DUMPIT and DUMPAB are very similar in function; they differ primarily in the type of output they produce.

4.8.3.1 Operating Procedures – Neither dump program will punch leader or trailer tape, but DUMPAB will always punch ten blank frames of tape at the start of each block of data dumped.

The operating procedures for both dump programs follow:

1. Select the dump program desired and place it in the reader specified by location XX7776 (Paragraph 4.8.1).

2. If a bootstrap tape is selected, load it using the Bootstrap Loader (Paragraph 4.8.1.2). When the computer halts, go to Step 4.

3. If an absolute binary tape is selected, load it using the Absolute Loader (Paragraph 4.8.2.2), relocating as desired.

   Place the proper start address in the Switch Register, press LOAD ADRS and START switches. (The start addresses are shown in Paragraph 4.8.3.3.)

4. When the computer halts, enter the address of the desired output device status register in the Switch Register and press CONT switch (low speed punch and teleprinter = 177564; high speed punch = 177554; line printer = 177514).

5. When the computer halts, enter in the Switch Register the address of the first byte to be dumped and press CONT switch. This address must be even when using DUMPIT.

6. When the computer halts again, enter in the Switch Register the address of the last byte to be dumped and press CONT switch. When using the low speed punch, set the punch to ON before pressing CONT switch.

7. Dumping will now proceed on the selected output device.

8. When dumping is complete, the computer will halt.

If further dumping is desired, proceed to Step 5. It is not necessary to respecify the output device address except when changing to another output device. In such a case, proceed to the second paragraph of Step 3 to restart.

If DUMPAB is being used, a transfer block must be generated as described below. If a tape read by the Absolute Loader does not have a transfer block, the loader will wait in an input loop. In such a case, the program may be

manually initiated, however, this practice is not recommended because there is no guarantee that load errors will not occur when the end of the tape is read.

The transfer block is generated by performing Step 5 with the transfer address in the Switch Register, and Step 6 with the transfer address minus 1 in the Switch Register. If the tape is not to be self-starting, an odd-numbered address must be specified in Step 5 (e.g., 000001).

The dump programs use all eight general registers and do not restore their original contents. Therefore, after a dump, the general registers should be loaded as necessary prior to their use by subsequent programs.

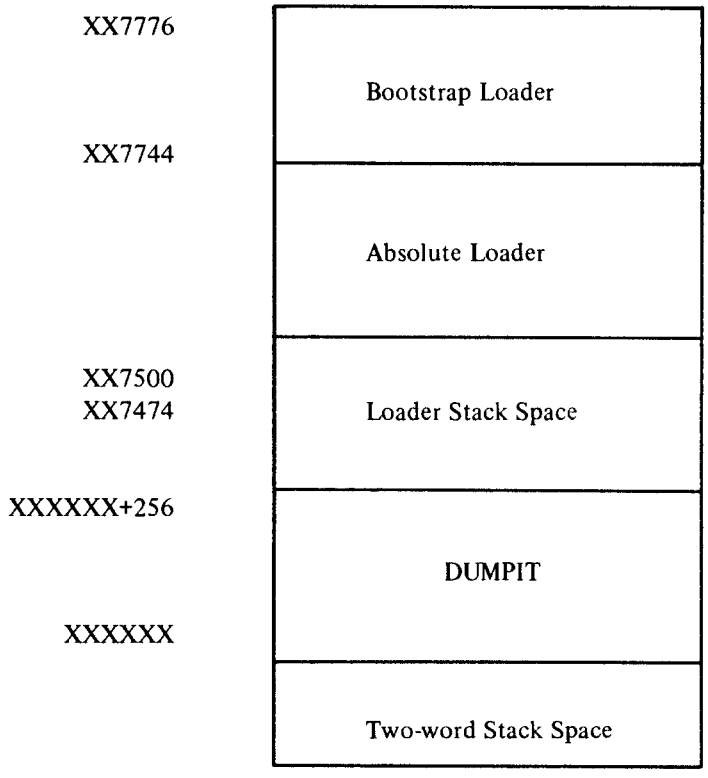
4.8.3.2 Output Formats – The octal output from DUMPIT is in the following format:

XXXXXX>YYYYYY YYYYYY YYYYYY YYYYYY YYYYYY YYYYYY

Where XXXXXX is the address of the first location printed or punched, and YYYYYY are words of data, the first of which starts at location XXXXXX. This is the format for every line of output. There are only eight words of data per line, but there can be as many lines as needed to complete the dump.

The output from DUMPAB is in absolute binary.

4.8.3.3 Storage Maps – The DUMPIT program is 87 words long. When used in absolute format, the storage map is as shown in Figure 4-4.



XXXXXX= desired load address = start address

Figure 4-4 Absolute Format

When used in bootstrap format, the storage map is as shown in Figure 4-5.

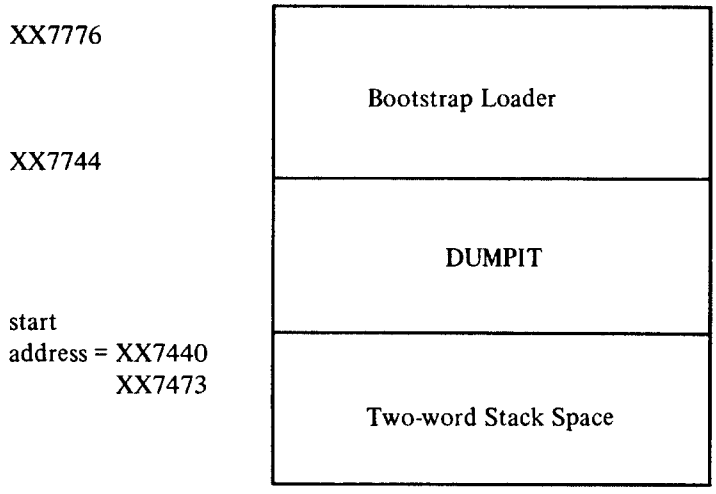


Figure 4-5 Bootstrap Format

PART 2

KD11–B PROCESSOR

Part 2 has been revised to reflect hardware changes to the KD11-B Processor. Chapter 5 has been revised but Chapter 6 remains as it was in the earlier edition. Chapters 7, 8, 9, and 10 have been deleted from this manual. Current versions of Chapters 7, 8, 9, and 10 are available in the KD11-B Processor Maintenance Manual, DEC-11-HKDBB-A-D. The former chapter structure of Part 2 was:

Chapter 5 – Processor General Description
Chapter 6 – Instruction Set
Chapter 7 – Console Description
Chapter 8 – KD11-B Detailed Description
Chapter 9 – Microprogram Control
Chapter 10 – KD11-B and Console Maintenance

CHAPTER 5
PROCESSOR GENERAL DESCRIPTION

5.1 KD11-B DEFINITION

Physically the KD11-B consists of two 8-1/2 by 15 inch modules, the M7260 and M7261. Each module contains approximately 100 dual in-line integrated circuits of the 14-, 16-, and 24-pin variety. There is one MOS-LSI 40-pin integrated circuit used on the M7260. This MOS circuit is the serial communication line (SCL) receiver and transmitter. All other integrated circuits used on the KD11-B are bipolar. The connections between the two modules are made through the backplane.

The KD11-B programmer's console interfaces to the processor via a 40-conductor cable that is attached to the M7260 module. The console is described in detail in the KD11-B Processor Maintenance Manual, DEC-11-HKDBB-A-D.

5.2 KD11-B AND THE UNIBUS

The processor is interfaced with memory and most peripherals by the Unibus as shown in Figure 5-1. The KD11-B is capable of arbitrating bus requests (BR) and non-processor requests (NPR) as they are asserted onto the Unibus by the connected peripherals.

The line clock and the serial communications line (SCL) do not interface with the processor via the Unibus in the traditional PDP-11 sense; both connect to the KD11-B through an internal bus. For most programs, these peripherals are indistinguishable from their appearance on other PDP-11 implementations. In other words, the program may access the line clock and the serial communications line by using instructions that move data to and from the Unibus address specified for these peripheral options in the *PDP-11 Peripherals Handbook.* These Unibus addresses are as follows:

a. Line Clock Status Register Address = 177546
b. SCL Receiver Status Register Address = 177560
c. SCL Receiver Buffer Register Address = 177562
d. SCL Transmitter Status Register Address = 177564
e. SCL Transmitter Buffer Register Address = 177566

It is not possible for the line clock and SCL to be addressed by any devices attached to the Unibus other than the KD11-B processor. For example, it is not possible to perform NPRs to the SCL from another peripheral such as the DECtape unit.

The SCL input/output is available for connection to such devices as the LA30 DECwriter, the VT05 CRT Terminal, or the Model 33 ASR Teletype. These SCL input/output signals interface at the fingers of the processor's M7260 module via a Berg connector located on the rear of the computer chassis as shown in Chapter 3.

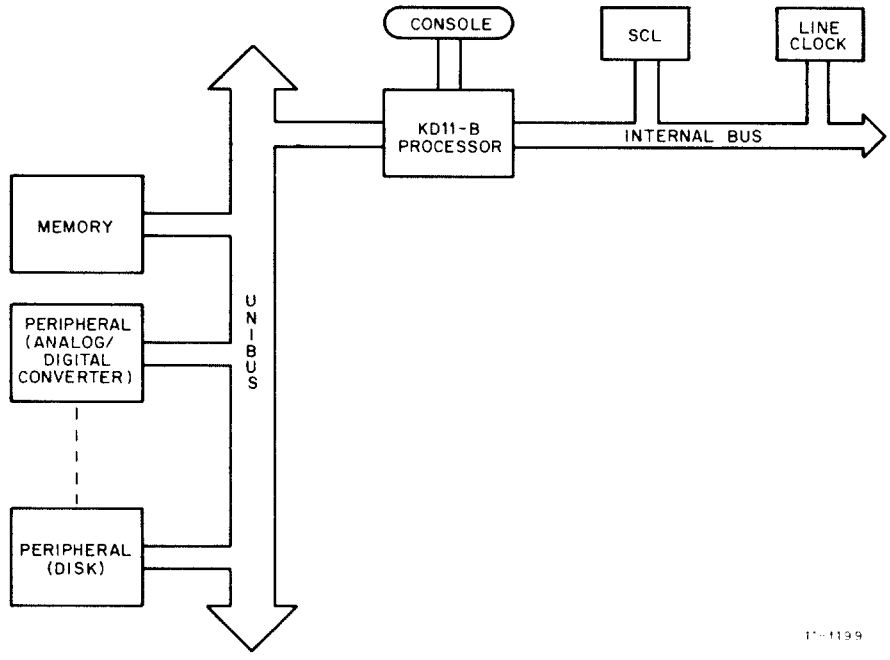


Figure 5-1 KD11-B With Interconnections to Memory and Peripherals

5.3 KD11-B AS AN INSTRUCTION INTERPRETER

Figure 5-2 illustrates the division of the KD11-B into Unibus control and instruction interpreter. This division is significant because in the KD11-B the Unibus control is implemented as a block of logic that is relatively independent of the rest of the processor.

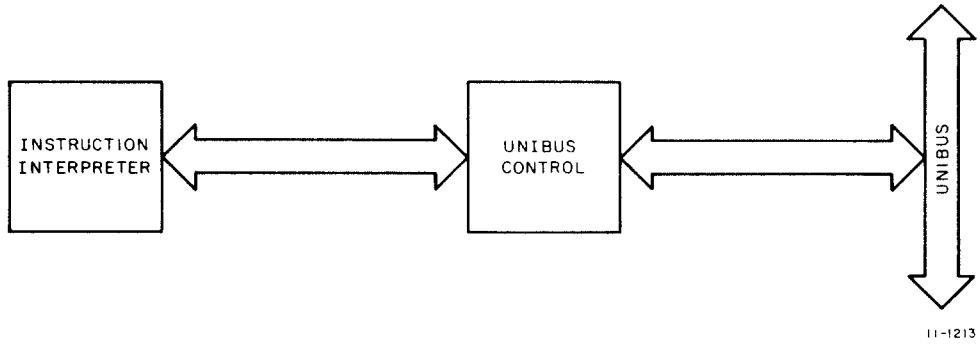


Figure 5-2 KD11-B Processor Block Diagram

In Figure 5-3, the instruction interpreter is further divided into a data path (DP), a data path control (DPC), and a control store (CS). Whenever power is applied to the computer, the DPC continually executes a program that is stored in the CS. All instructions, interrupt sequences, and console functions are performed by the DPC when executing a microprogram contained in the CS. The Unibus control and the DP are facilities used by the DPC in the course of performing its tasks. The program contained in the CS is referred to as the microprogram.

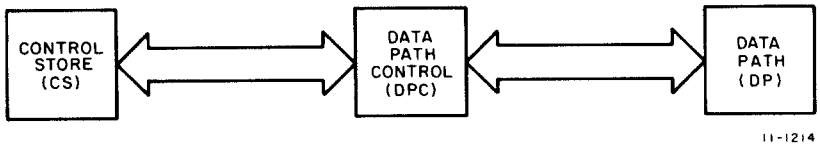


Figure 5-3 Instruction Interpreter Block Diagram

5.4 MEDIUM AND LARGE SCALE INTEGRATED CIRCUIT REPRESENTATIONS

MSI and LSI integrated circuits (Figure 5-4) are represented in the KD11-B print set as rectangles with inputs on the left and outputs on the right. Control lines often enter the IC from the bottom. The functional descriptions of the KD11-B MSI and LSI ICs are contained in Appendix A.

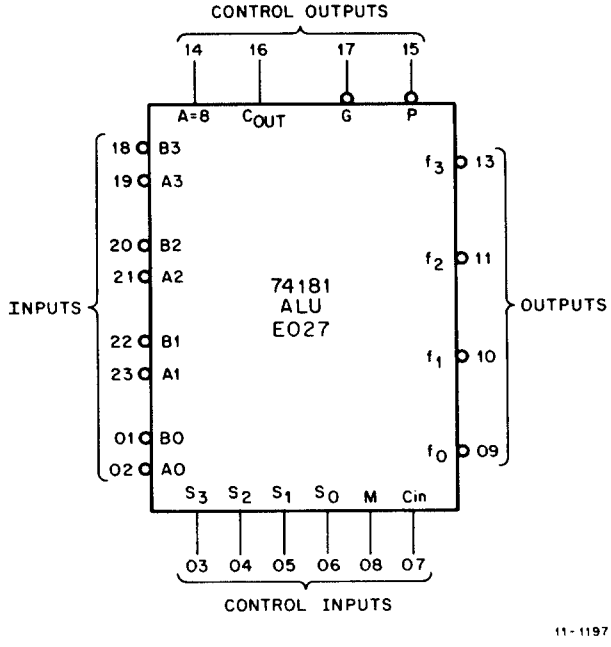


Figure 5-4 ALU, MSI Circuit Type 74181 Representation

5.4.1 Microprogram Documentation

The microprogram is documented at three levels in the print set. The first level is the microprogram flow listing (K-MP-KDN-B-1), at this level, the microprogram is described in terms of register transfers. The microprogram symbolic listing (K-MP-KD11-B-2) shows how the microprogram accomplishes each step. (References in the microprogram listing are symbolic; e.g., scratch pad address = R7.) The binary equivalent is shown in the microprogram binary listing (K-MP-KD11-B-3), which actually shows the binary contents of each word of the microprogram. The microprogram cross reference listing lists the microprogram by address (K-MP-KD11-B-4). The microprogram is discussed in detail in the KD11-B Processor Maintenance Manual, DEC-11-HKDBB-A-D.

5.4.2 Read-Only Memory (ROM) Maps

Figure 5-5 is a typical ROM map listing. ROM map listings for the ROMs used in the KD11-B processor are provided in the *Engineering Drawing Manual* (K-RL-M7260-8 and K-RL-M7261-8).

```
                                        /( =Y8 (PIN #9) CONA INT TRAN SYNC L
                                        †/( =Y7 (PIN #7) CONA REG ADDR L
                                        ††/( =Y6 (PIN #6) CONA RECEIVE L
                                        †††/( =Y5 (PIN #5) CONA TRANSMIT L
                                        ††††/( =Y4 (PIN #4) CONA LOAD MODEM PSW L
                                        †††††/( =Y3 (PIN #3) CONA LOAD L CLK PSW L
                                        ††††††/( =Y2 (PIN #2) CONG SP WRITE L
                                        †††††††/( =Y1 (PIN #1) CONG LOAD PSW L
  OCTAL  DECIMAL                        †††††††          OCTAL
ADDRESS ADDRESS    EDCBA                †††††††          DATA
   000       0     00000   11111111          377
   001       1     00001   11111111          377
   002       2     00010   11111111          377
   003       3     00011   11111111          377
   004       4     00100   01111110          176   PSW .TRAN OUT BA=177776
   005       5     00101   11111111          377   PSW .TRAN OUT,BAR
   006       6     00110   01111011          173   LCLK .TRANOUT
   007       7     00111   11111111          377   LCLK .TRANOUT,BAR
   010       8     01000   00111101          075   GR<R0:R17> .TRANOUT BA=1777XX
   011       9     01001   10111111          277   GR<R0:R17> .TRANOUT.BAR
   012      10     01010   01111111          177   ODD BYTE (LCLK/TK/TP)
   013      11     01011   11111111          377
   014      12     01100   11111111          377
   015      13     01101   11111111          377
   016      14     01110   01111111          177   SWR .TRANOUT BA=177570
   017      15     01111   11111111          377   SWR .TRANOUT,BAR
   020      16     10000   01101111          127   TKS .TRANOUT BA=177560
   021      17     10001   11011111          337   TKS .TRANOUT,BAR
   022      18     10010   01100111          147   TPS .TRANOUT BA=177564
   023      19     10011   11101111          357   TPS .TRANOUT,BAR
   024      20     10100   01011111          137   TKB .TRANOUT BA=177562
   025      21     10101   11011111          337   TKB .TRANOUT,BAR
   026      22     10110   01101111          157   TPB .TRANOUT BA=177566
   027      23     10111   11101111          357   TPB .TRANOUT,BAR
   030      24     11000   11111111          377
   031      25     11001   11111111          377
   032      26     11010   11111111          377
   033      27     11011   11111111          377
   034      28     11100   11111111          377
   035      29     11101   11111111          377
   036      30     11110   11111111          377
   037      31     11111   11111111          377
                   †††††
                   ††††/( A(PIN #10) IS  CONA TRAN OUT L
                   †††/( B(PIN #11) IS  Y3 OF F025
                   ††/( C(PIN #12) IS  Y2 OF F025
                   †/( D(PIN #13) IS  Y1 OF F025
                   /( E(PIN #14) IS  Y4 OF F025
```

Figure 5-5 E068 ROM Map Example

CHAPTER 6
INSTRUCTION SET

6.1 INTRODUCTION

The KD11-B is defined by its instruction set. The sequences of processor operations are selected according to the instruction decoding. This chapter contains tables that describe the PDP-11 instructions and instruction set addressing modes. Instruction set differences between the PDP-11/05, 11/10 and PDP-11/20 are listed in Table 6-8.

6.2 ADDRESSING MODES

6.2.1 Introduction

Data stored in memory must be accessed and manipulated. Data handling is specified by a PDP-11 instruction (MOV, ADD, etc.) which usually indicates:

a. The function (operation code).

b. A general purpose register for locating the source operand and/or a general purpose register for locating the destination operand.

c. An addressing mode [to specify how the selected register(s) is to be used].

A large portion of the data handled by a computer is usually structured in character strings, arrays, lists, etc. Thus, the PDP-11 is designed to handle structured data efficiently and flexibly. The general registers may be used with an instruction in any of the following ways:

a. As accumulators. The data to be manipulated resides within the register.

b. As pointers. The contents of the register are the address of the operand, rather than the operand itself.

c. As pointers that automatically step through core locations. Automatically stepping forward through consecutive core locations is termed autoincrement addressing; automatically stepping backwards is termed autodecrement addressing. These modes are particularly useful for processing tabular data.

d. As index registers. In this instance, the contents of the register and the word following the instruction are summed to produce the address of the operand. This allows easy access to variable entries in a list.

PDP-11s also have instruction addressing mode combinations that facilitate temporary data storage structures for convenient handling of data that must be frequently accessed. This is known as the "stack".

In the PDP-11 any register can be used as a stack pointer under program control; however, certain instructions associated with subroutine linkage and interrupt service automatically use register 6 as a hardware stack pointer. For this reason, R6 is frequently referred to as the SP.

Two types of instructions utilize the addressing modes: single operand and double operand. Figure 6-1 shows the formats of these two types of instructions. The addressing modes are listed in Table 6-1.

6.2.2 Instruction Timing

The PDP-11 is an asynchronous processor in which, in many cases, memory and processor operations are overlapped. The execution time for an instruction is the sum of a basic instruction time and the time to determine and fetch the source and/or destination operands. Table 6-2 shows the addressing times required for the various modes of addressing source and destination operands. All times stated are subject to ±10% variation.

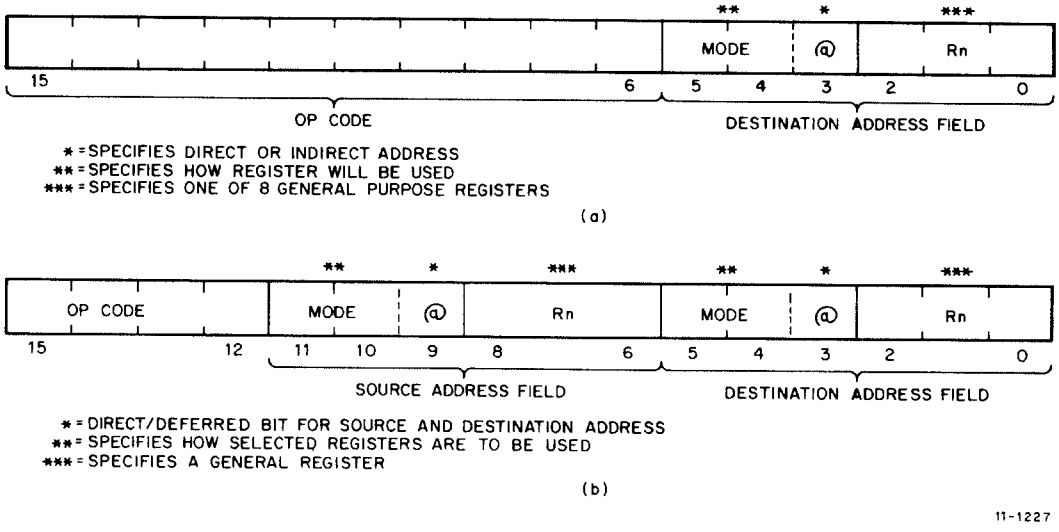


Figure 6-1 Addressing Mode Instruction Formats

6.3 PDP-11/05 INSTRUCTIONS

The PDP-11 instructions can be divided into five groupings:

a. Single Operand Instructions (shifts, multiple precision instructions, rotates)
b. Double Operand Instructions (arithmetic and logical instructions)
c. Program Control Instructions (branches, subroutines, traps)
d. Operate Group Instructions (processor control operations)
e. Condition Codes Operators (processor status word bit instructions)

Tables 6-3 through 6-7 list each instruction, including byte instructions for the respective instruction groups. Figure 6-2 shows the six different instruction formats of the instruction set, and the individual instructions in each format.

6.4 INSTRUCTION SET DIFFERENCES

Table 6-8 lists the differences between the PDP-11/20 and PDP-11/05 instruction sets.

Table 6-1
Addressing Modes

Binary Code	Name	Assembler Syntax	Function
		DIRECT MODES	
000	Register	Rn	Register contains operand.
010	Autoincrement	(Rn) +	Register contains address of operand. Register contents incremented after reference.
100	Autodecrement	-(Rn)	Register contents decremented before reference register contains address of operand.
110	Index	X(Rn)	Value X (stored in a word following the instruction) is added to (Rn) to produce address of operand. Neither X nor (Rn) are modified.
		DEFERRED MODES	
001	Register Deferred	@Rn or (Rn)	Register contains the address of the operand.
011	Autoincrement Deferred	@(Rn) +	Register is first used as a pointer to a word containing the address of the operand, then incremented (always by two; even for byte instructions).
101	Autodecrement	@-(Rn)	Register is decremented (always by two; even for byte instructions) and then used as a pointer to a word containing the address of the operand.
111	Index Deferred	@X(Rn)	Value X (stored in a word following the instruction) and (Rn) are added and the sum is used as a pointer to a word containing the address of the operand. Neither X nor (Rn) are modified.
		PC ADDRESSING	
010	Immediate	#n	Operand follows instruction.
011	Absolute	@#A	Absolute address follows instruction.
110	Relative	A	Address of A, relative to the instruction, follows the instruction.
111	Relative Deferred	@A	Address of location containing address of A, relative to the instruction, follows the instruction.

Rn = Register
X, n, A = next program counter (PC) word (constant)

Table 6-2
Addressing Times

	Addressing Format		Time (μs)	
Mode	**Description**	**Symbolic**	**Source***	**Destination****
0	Register	R	0	0
1	Register Deferred	@R or (R)	0.9	2.4
2	Autoincrement	(R) +	0.9	2.4
3	Autoincrement Deferred	@(R) +	2.4	3.4
4	Autodecrement	- (R)	0.9	2.4
5	Autodecrement Deferred	@ - (R)	2.4	3.4
6	Indexed	± X (R)	2.4	3.4
7	Index Deferred	@ ± X (R) or @ (R)	3.4	4.7

* For Source time, add 1.3 μs for odd byte addressing.
** For destination time, modify as follows:

a. Add 1.3 μs for odd byte addressing with a non-modifying instruction.

b. Add 2.4 μs for odd byte addressing with a modifying instruction.

c. Subtract 1.2 μs for a non-modifying instruction.

Table 6-3
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
CLR CLRB 3.4 μs	0050DD* 1050DD	(dst)† ← 0	N: cleared Z: set V: cleared C: cleared	Contents of specified destination are replaced with zeroes.
COM COMB 3.4 μs	0051DD 1051DD	(dst) ← n (dst)	N: set if most significant bit of result is 0 Z: set if result is 0 V: cleared C: set	Replaces the contents of the destination address by their logical complement (each bit equal to 0 set and each bit equal to 1 cleared).
INC INCB 3.4 μs	0052DD 1052DD	(dst) ← (dst) + 1	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) was 077777 C: not effected	Add 1 to the contents of the destination.
DEC DECB 3.4 μs	0053DD 1053DD	(dst) ← (dst) - 1	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) was 100000 C: not effected	Subtract 1 from the contents of the destination.
NEG NEGB 3.4 μs	0054DD 1054DD	(dst) ← -(dst)	N: set if result is less than 0 Z: set if result is 0 V: set if result is 100000 C: cleared if result is 0	Replaces the contents of the destination address by its 2's complement. Note that 100000 is replaced by itself.
ADC ADCB 3.4 μs	0055DD 1055DD	(dst) ← (dst) + C	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) is 077777 and C is 1 C: set if (dst) is 177777 and C is 1	Adds the contents of the C-bit into the destination. This permits the carry from the addition of the low order words/bytes to be carried into the high order result.

Table 6-3 (Cont)
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
SBC SBCB 3.4 μs	0056DD 1056DD	(dst) ← (dst) -C	N: set if result is less than 0 Z: set if result is 0 V: set if (dst) was 100000 C: cleared if (dst) is 0 and C is 1	Subtracts the contents of the C-bit from the destination. This permits the carry from the subtraction of the low order words/ bytes to be subtracted from the high order part of the result.
TST TSTB 3.4 μs	0057DD 1057DD	(dst) ← (dst)	N: set if result is less than 0 Z: set if result is 0 V: cleared C: cleared	Sets the condition codes N and Z according to the contents of the destination address.
ROR RORB 3.4 μs	0060DD	(dst) ← (dst) rotate right one place.	N: set if high order bit of the result is set Z: set if all bits of result are 0 V: loaded with the exclusive-OR of the N-bit and the C-bit as set by ROR	Rotates all bits of the destination right one place. The low order bit is loaded into the C-bit and the previous contents of the C-bit are loaded into the high order bit of the destination.
ROL ROLB 3.4 μs	0061DD 1061DD	(dst) ← (dst) rotate left one place.	N: set if the high order bit of the result word is set (result < 0); cleared otherwise Z: set if all bits of the result word = 0; cleared otherwise V: loaded with the exclusive-OR of the N-bit and C-bit (as set by the completion of the rotate operation) C: loaded with the high order bit of the destination	Rotate all bits of the destination left one place. The high order bit is loaded into the C-bit of the status word and the previous contents of the C-bit are loaded into the low order bit of the destination.

Table 6-3 (Cont)
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
ASR ASRB 3.4 μs	0062DD 1062DD	(dst) ← (dst) shifted one place to the right.	N: set if the high order bit of the result is set (result < 0); cleared otherwise Z: set if the result = 0; cleared otherwise V: loaded from the exclusive-OR of the N-bit and C-bit (as set by the completion of the shift operation). C: loaded from low order bit of the destination	Shifts all bits of the destination right one place. The high order bit is replicated. The C-bit is loaded from the low order bit of the destination. ASR performs signed division of the destination by two.
ASL ASLB 3.4 μs	0063DD 1063DD	(dst) ← (dst) shifted one place to the left.	N: set if high order bit of the (result < 0); cleared otherwise Z: set if the result = 0; cleared otherwise V: loaded with the exclusive-OR of the N-bit and C-bit and C-bit (as set by the completion of the shift operation) C: loaded with the high order bit of the destination	Shifts all bits of the destination left one place. The low order bit is loaded with a 0. The C-bit of the status word is loaded from the high order bit of the destination. ASL performs a signed multiplication of the destination by 2 with overflow indication.

Table 6-3 (Cont)
Single Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
JMP 1.0 μs	0001DD	PC ← (dst)	Not effected.	JMP provides more flexible program branching than provided with the branch instruction. Control may be transferred to any location in memory (no range limitation) and can be accomplished with the full flexibility of the addressing modes, with the exception of register mode 0. Execution of a jump with mode 0 will cause an illegal instruction condition. (Program control cannot be transferred to a register.) Register deferred mode is legal and will cause program control to be transferred to the address held in the specified register. Note that instructions are word data and must therefore be fetched from an even numbered address. A boundary error trap condition will result when the processor attempts to fetch an instruction from an odd address.
SWAB 4.3 μs	0003DD	Byte 1/Byte 0 Byte 0/Byte 1	N: set if high order bit of low order byte (bit 7) of result is set, cleared otherwise Z: set if low order byte of result = 0; cleared otherwise V: cleared C. cleared	Exchanges high order byte and low order byte of the destination word (destination must be a word address).

* DD = destination (address mode and register)
† (dst) = destination contents

Table 6-4
Double Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
MOV MOVB 3.7 μs 3.1 μs mode 0	01SSDD* 11SSDD	(dst) ← (src) †	N: set if (src) < 0; cleared otherwise Z: set if (src) = 0; cleared otherwise V: cleared C: not effected	Word: Moves the source operand to the destination location. The previous contents of the destination are lost. The source operand is not effected. Byte: Same as MOV. The MOVB to a resistor (unique among byte instructions) extends the most significant bit of the low order byte (sign extension). Otherwise MOVB operates on bytes exactly as MOV operates on words.
CMP CMPB 3.7 μs	02SSDD 12SSDD	(src) - (dst) [in detail, (src) + ~ (dst) + 1]	N: set if result < 0, cleared otherwise Z: set if result = 0; cleared otherwise V: set if there was arithmetic overflow, i.e., operands were of opposite signs and the sign of the destination was the same as the sign of the result; cleared otherwise C: cleared if there was a carry from the most significant bit of the result; set otherwise	Compares the source and destination operands and sets the condition codes, which may then be used for arithmetic and logical conditional branches. Both operands are uneffected. The only action is to set the condition codes. The compare is customarily followed by a conditional branch instruction. Note that unlike the subtract instruction the order of operation is (src) - (dst), not (dst) - (src).

Table 6-4 (Cont)
Double Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BIT BITB 3.7 μs	03SSDD 13SSDD	(src) $\wedge$ (dst)	N: set if high order bit of result set; cleared otherwise Z: set if result = 0; cleared otherwise V: cleared C: not effected	Performs logical AND comparison of the source and destination operands and modifies condition codes accordingly. Neither the source nor destination operands are effected. The BIT instruction may be used to test whether any of the corresponding bits that are set in the destination are clear in the source.
BIC BICB 3.7 μs	04SSDD 14SSDD	(dst) $\leftarrow \sim$ (src) $\wedge$ (dst)	N: set if high order bit of result set, cleared otherwise Z: set if result = 0, cleared otherwise V: cleared C. not effected	Clears each bit in the destination that corresponds to a set bit in the source. The original contents of the destination are lost. The contents of the source are uneffected.
BIS BISB 3.7 μs	05SSDD 15SSDD	(dst) $\leftarrow$ (src) $\wedge$ (dst)	N: set if high order bit of result set; cleared otherwise Z: set if result = 0; cleared otherwise V: cleared C: not effected	Performs inclusive-OR operation between the source and destination operands and leaves the result at the destination address; i.e., corresponding bits set in the destination. The contents of the destination are lost.
ADD	06SSDD	(dst) $\leftarrow$ (src) + (dst)	N: set if result 0; cleared otherwise Z: set if result = 0; cleared otherwise	Adds the source operand to the destination operand and stores the result at the destination address. The original contents of the destination are lost. The contents of the source are not effected. Two's complement addition is performed.

Table 6-4 (Cont)
Double Operand Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
ADD (Cont)			V: set if there was arithmetic overflow as a result of the operation; that is both operands were of the same sign and the result was of the opposite sign; cleared otherwise C: set if there was a carry from the most significant bit of the result cleared otherwise	
SUB 3.7 μs	16SSDD	(dst) ← (dst) - (src) in detail, (dst) + ~ (src) + 1 (dst)	N: set if result < 0; cleared otherwise Z: set if result = 0; cleared otherwise V: set if there was arithmetic overflow as a result of the operation. i.e., if operands were of opposite signs and the sign of the source was the same as the sign of the result, cleared otherwise C: cleared if there was a carry from the most significant bit of the result; set otherwise	Subtracts the source operand from the destination operand and leaves the result at the destination address. The original contents of the destination are lost. The contents of the source are not effected. In double precision arithmetic, the C-bit, when set, indicates a borrow.

* SS = source (address mode and register)
† (src) = source contents

Table 6-5
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BR 2.5 μs	000400 xxx†	PC ← PC + (2 X offset)	Uneffected	Provides a way of transferring program control within a range of -128 to +127 words with a one word instruction. It is an unconditional branch.
BNE 1.9 μs no branch 2.5 μs branch	001000 xxx	PC ← PC + (2 X offset) if Z = 0	Uneffected	Tests the state of the Z-bit and causes a branch if the Z-bit is is clear. BNE is the complementary operation to BEQ. It is used to test inequality following a CMP, to test that some bits set in the destination were also in the source, following a BIT, and generally, to test that the result of the previous operation was not 0.
BEQ 1.9 μs no branch 2.5 μs branch	001400 xxx	PC ← PC + (2 X offset) if Z = 1	Uneffected	Tests the state of the Z-bit and causes a branch if Z is set. As an example, it is used to test equality following a CMP operation, to test that no bits set in the destination were also set in the source following a BIT operation, and generally, to test that the result of the previous operation was 0.
BGE 1.9 μs no branch 2.5 μs branch	002000 xxx	PC ← PC + (2 X offset) if N v V = 0	Uneffected	Causes a branch if N and V are either both clear or both set. BGE is the complementary operation to BLT. Thus, BGE always causes a branch when it follows an operation that caused addition to two positive numbers. BGE also causes a branch on a 0 result.

Table 6-5 (Cont)
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BLT 1.9 μs no branch 2.5 μs branch	002400 xxx	PC ← PC + (2 X offset) if N V = 1	Uneffected	Causes a branch if the exclusive-OR of the N- and V-bits are 1. Thus, BLT always branches following an operation that added two negative numbers, even if overflow occurred. In particular, BLT always causes a branch if it follows a CMP instruction operating on a negative source and a positive destination (even if overflow occurred). Further, BLT never causes a branch when it follows a CMP instruction operating on a positive source and negative destination. BLT does not cause a branch if the result of the previous operation was 0 (without overflow).
BGT 1.9 μs no branch 2.5 μs branch	003000 xxx	PC ← PC + (2 X offset) if Z v (N⊻ V) = 0	Uneffected	Operation of BGT is similar to BGE, except BGT does not cause a branch on a 0 result.
BLE 1.9 μs no branch 2.5 μs branch	003400 xxx	PC ← PC + (2 X offset) if Z v (N⊻V) = 1	Uneffected	Operation is similar to BLT but in addition will cause a branch if the result of the previous operation was 0.
BPL 1.9 μs no branch 2.5 μs branch	100000 xxx	PC ← PC + (2 X offset) if N = 0	Uneffected	Tests the state of the N-bit and causes a branch if N is clear. BPL is the complementary operation of BMI.
BMI 1.9 μs no branch 2.5 μs branch	100400 xxx	PC ← PC + (2 X offset) if N = 1	Uneffected	Tests the state of the N-bit and causes a branch if N is set. It is used to test the sign (most significant bit) of the result of the previous operation.

Table 6-5 (Cont)
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
BHI 1.9 μs no branch 2.5 μs branch	101000 xxx	PC ← PC + (2 X offset) if C = 0	Uneffected	Causes a branch if the previous operation causes neither a carry nor a 0 result. This will happen in comparison (CMP) operations as long as the source has a higher unsigned value than the destination.
BLOS 1.9 μs no branch 2.5 μs branch	101400 xxx	PC ← PC + (2 X offset) if C v Z = 1	Uneffected	Causes a branch if the previous operation caused either a carry or a 0 result. BLOS is the complementary operation to BHI. The branch occurs in comparison operations as long as the source is equal to or has a lower unsigned value than the destination. Comparison of unsigned values with the CMP instruction to be tested for "higher or same" and "higher" by a simple test of the C-bit.
BVC 1.9 μs no branch 2.5 μs branch	102000 xxx	PC ← PC + (2 X offset) if V = 0	Uneffected	Tests the state of the V-bit and causes a branch if the V-bit is clear. BVC is complementary operation to BVS.
BVS 1.9 μs no branch 2.5 μs branch	102400 xxx	PC ← PC + (2 X offset) if V = 1	Uneffected	Tests the state of V-bit (overflow) and causes a branch if the V-bit is set. BVS is used to detect arithmetic overflow in the previous operation.
BCC BHIS 1.9 μs no branch 2.5 μs branch	103000 xxx	PC ← PC + (2 X offset) if C = 0	Uneffected	Tests the state of the C-bit and causes a branch if C is clear. BCC is the complementary operation to BCS.
BCS BLO 1.9 μs no branch 2.5 μs branch	103400 xxx	PC ← PC + (2 X offset) if C = 1	Uneffected	Tests the state of the C-bit and causes a branch if C is set. It is used to test for a carry in the result of a previous operation.

Table 6-5 (Cont)
Program Control Instruction

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
JRS 3.8 μs	004RDD	(tmp) ← (dst) (tmp is an internal processor register) ↓ (SP) ← reg (push reg contents onto processor stack) reg ← PC PC holds location following JSR; this address PC ← (tmp), now put in (reg)	Uneffected	In execution of the JSR, the old contents of the specified register (the linkage pointer) are automatically pushed onto the processor stack and new linkage information placed in the register. Thus, subroutines nested within subroutines to any depth may all be called with the same linkage register. There is no need either to plan the maximum depth at which any particular subroutine will be called or to include instructions in each routine to save and restore the linkage pointer. Further, since all linkages are saved in a re-entrant manner on the processor stack. execution of a subroutine may be interrupted, and the same subroutine re-entered and executed by an interrupt service routine. Execution of the initial subroutine can then be resumed when other requests are satisfied. This process (called nesting) can proceed to any level. JSR PC, dst is a special case of the PDP-11 subroutine call suitable for subroutine calls that transmit parameters.
RTS 3.8 μs	00020R	PC ← (reg) (reg) ← SP ↑	Uneffected	Loads contents of register into PC and pops the top element of the processor stack into the specified register. Return from a non-re-entrant subroutine is typically made through the same register that was used in its call. Thus, a subroutine called with a JSR PC, dst exits with an RTS PC, and a subroutine called with a JSR R5, dst may pick up parameters with addressing modes (R5) +, X (R5), or @X (R5) and finally exit, with an RTS R5.

Table 6-5 (Cont)
Program Control Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
(No mnemonic) 8.2 μs	000003	↓ (SP) ← PS ↓ (SP) ← PC PC ← (14) PS ← (16)	N: loaded from trap vector Z: loaded from trap vector V: loaded from trap vector C: loaded from trap vector	Performs a trap sequence with a trap vector address of 14. Used to call debugging aids. The user is cautioned against employing code 000003 in programs run under these debugging aids.
IOT 8.2 μs	000004	↓ (SP) ← PS ↓ (SP) ← PC PC ← (20) PS ← (22)	N: loaded from trap vector Z: loaded from trap vector C: loaded from trap vector	Performs a trap sequence with a trap vector address of 20. Used to call the I/O executive routine IOX in the paper-tape software system, and for error reporting in the disk operating system.
EMT 8.2 μs	104000	↓ (SP) ← PS ↓ (SP) ← PC PC ← (30) PS ← (32)	N: loaded from trap vector Z: loaded from trap vector V: loaded from trap vector C: loaded from trap vector	All operation codes from 104000 to 104377 are EMT instructions and may be used to transmit information to the emulating routine (e.g., function to be performed). The trap vector for EMT is at address 30; the new central processor status (PS) is taken from the word at address 32. **CAUTION** **EMT is used frequently by DEC system software and is therefore not recommended for general use.**
TRAP 8.2 μs	104400 to 104777	↓ (SP) ← PS ↓ (SP) ← PC PC ← (34) PS ← (36)	N: loaded from trap vector Z: loaded from trap vector V: loaded from trap vector C: loaded from trap vector	Operation codes from 104400 to 104777 are TRAP instructions TRAPs and EMTs are identical in operation, except that the trap vector for TRAP is at address 34. **NOTE** **Since DEC software makes frequent use of EMT, the TRAP instruction is recommended for general use.**

NOTE: Condition Codes are uneffected by these instructions

†xxx = offset, 8 bits (0-7) of instruction format
R = register (linkage pointer)

Table 6-6
Operate Group Instructions

Mnemonic/ Instruction Time	OP Code	Operation	Condition Codes	Description
HALT 1.8 μs	000000		Not effected	Causes the processor operation to cease. The console is given control of the processor. The console data lights display the address of the HALT instruction plus two. Transfers on the Unibus are terminated immediately. The PC points to the next instruction to be executed. Pressing the CON key on the console causes processor operation to resume. No INIT signal is given.
WAIT 1.8 μs	000001		Not effected	Provides a way for the processor to relinquish use of the bus while it waits for an external interrupt. Having been given a WAIT command, the processor will not compete for bus by fetching instructions or operands from memory. This permits higher transfer rates between device and memory, since no processor induced latencies will be encountered by bus requests from the device. In WAIT, as in all instructions, the PC points to the next instruction following the WAIT operation. Thus, when an interrupt causes the PC and PS to be pushed onto the stack, the address of the next instruction following the WAIT is saved. The exit from the interrupt routine (i.e., execution of an RTI instruction) will cause resumption of the interrupted process at the instruction following the WAIT.
RTI 4.4 μs	000002	PC (SP) PSW (SP)	N: loaded from processor stack Z: loaded from processor stack V: loaded from processor stack C: loaded from processor stack	Used to exit from an interrupt or trap service routine. The PC and PSW are restored (popped) from the processor stack. If a trace trap is pending, the first instruction after the RTI will be executed prior to the next T trap.
RESET 20 ms	000005	PC (SP) PSW (SP)	Not effected	Sends INIT on the Unibus for 20 ms. All devices on the Unibus are reset to their state at power-up.

Table 6-7
Condition Code Operators

Mnemonic/ Instruction Time	OP Code	Description
CLC	000241	Set and clear condition code bits. Selectable combination of these bits may be cleared or set together. Condition code bits corresponding to bits in the condition code operator (bits 0–3) are modified according to the sense of bit 4, the set/clear bit of the operator; i.e., set the bit specified by bit 0, 1, 2, or 3 if bit 4 is a 1. Clear corresponding bits if bit 4 = 0.
CLZ	000242	
CLN	000244	
CLV	000250	
Set all CCs	000261	
Clear all CCs	000262	
Clear V and C	000264	
No operation	000270	
No operation	000277	
	000257	
2.5 μs	000243	
	000240	
	000260	

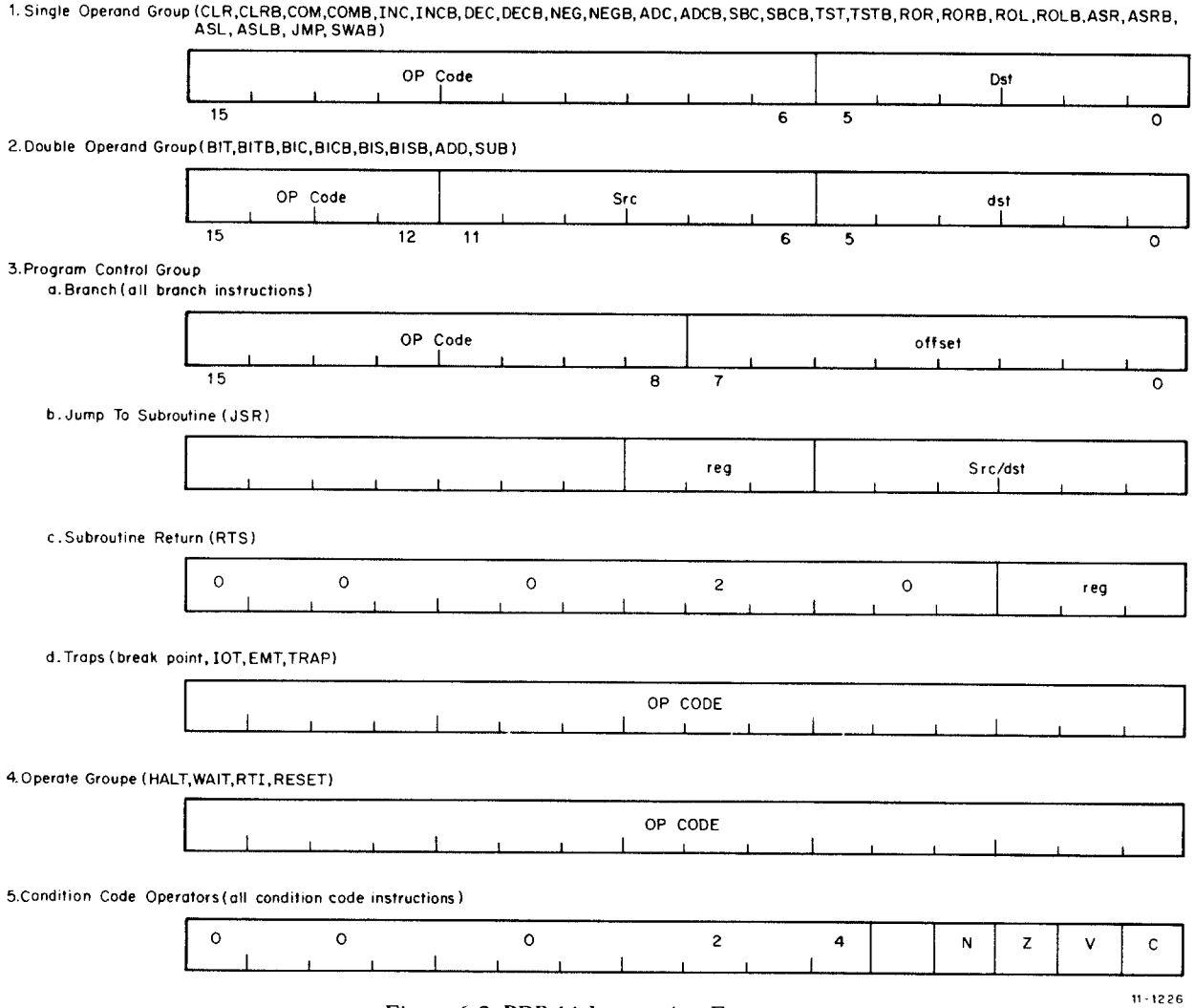


Figure 6-2 PDP-11 Instruction Formats

Table 6-8
PDP-11 Differences

PDP-11/15, PDP-11/20	PDP-11/05, PDP-11/10
OPR %R, (R) +/-(R), source operand is %R after autoincrement/autodecrement of DEST register only when source and destination registers are the same. Example: 12700 MOV # 100, R0 100 10020 MOV R0, (R0) + 0 HALT After Execution: R0 = 102 LOC100 = 102	OPR %R, (R) +/-R source operand is %R before autoincrement/autodecrement of DEST register whether source or destination registers are the same or not. Example: 12700 MOV #100, R0 100 10020 MOV R0, (R0) + 0 HALT After Execution: R0 = 102 LOC100 = 100 (Note that LOC100 is now 100)
OPR %R, @-(R) /@ (R) + uses R after autodecrement/autoincrement as source operand.	OPR %R, @-(R) /@ (R) + uses R before autodecrement/autoincrement as source operand.
MOV PC, LOC stores PC of INST +4 in LOC.	MOV PC, LOC stores PC of INST +2 in LOC.
SWAB does not change V.	Swab clears V.
Program halt displays PC of halt instruction in ADDRESS lights. DATA lights display (RO).	Displays next PC.
Byte ops to the odd byte of the PS cause odd address trap.	Byte ops to odd byte of PS do not trap. Not all bits may exist.
The RESET instruction clears the RUN light such that program loops that make frequent use of RESET may not appear to be running.	RESET does not clear the RUN light.
Power fail during RESET instruction is not recognized until after the instruction is finished (70 ms). Too late, so don't use RESET. RESET instruction consists of 70 ms pause with INIT occurring during first 20 ms.	Power fail immediately ends the RESET instructions and traps if an INIT is in progress (22 ms). A minimum INIT of 300 ns occurs if the instruction aborted. Power fail during RESET fetch is fatal: no power-down sequence.

Table 6-8 (Cont)
PDP-11 Differences

PDP-11/15, PDP-11/20	PDP-11/05, PDP-11/10
The first instruction in an interrupt service routine is guaranteed to be executed.	The first instruction in an interrupt routine will not be executed if another interrupt occurs at a higher priority level than was assumed by the first interrupt.
Sequence of internal processor traps, external interrupts, HALT and WAIT: BUS ERROR Trap Odd Address Data Time Out HALT Instruction for Console Operation TRAP Instructions: Illegal or Reserved Instructions, TRTT, IOT, EMT, TRAP TRACE TRAP: T-bit of processor status OVFL Trap: Stack overflow PWR FAIL Trap: Power down CONSOLE BUS REQUEST: Console operation after HALT switch UNIBUS BUS REQUEST: Peripheral Request, compared with Processor Priority - usually an interrupt occurs. WAIT LOOP: Loop on a WAIT instruction in IR until an interrupt allows exit. A CONSOLE BUS REQUEST returns to this loop after being honored.	Sequences: BUS ERROR Traps HALT Instruction TRAP Instructions OVFL Trap PWR Fail Trap UNIBUS BUS REQUESTS CONSOLE STOP (HALT switch) WAIT LOOP

PART 3

MM11–K AND MM11–L MEMORIES

Part 3 provides both general and detailed descriptions of the MM11-K and MM11-L core memories that are used in the PDP-11/05 and PDP-11/10. Maintenance information is also included. The chapters of Part 3 are:

CHAPTER 11
MM11-K AND L GENERAL DESCRIPTION

11.1 INTRODUCTION

This chapter provides the user with the theory of operation and logic diagrams necessary to understand and maintain the MM11-K and MM11-L Read/Write Core Memories. The level of discussion assumes that the reader is familiar with basic digital computer theory. Both general and detailed descriptions of the core memories are included.

Although memory control signals and data pass through the Unibus, it is beyond the scope of this discussion to describe the operation of the Unibus. A detailed description of the Unibus is presented in the *PDP-11 Peripherals Handbook.*

A complete set of engineering logic drawings is shipped with each core memory. These drawings are bound in a separate volume entitled *MM11-K and L Core Memories, Engineering Drawings.* The drawings reflect the latest print revisions and correspond to the specific memory shipped to the user.

11.2 GENERAL DESCRIPTION

This paragraph provides a physical description and specifications for the memory. The major functional units of each memory are briefly described, and the basic memory operations are discussed.

11.2.1 Physical Description

The MM11-K provides 4096 (4K) 16-bit words: the MM11-L provides 8192 (8K) 16-bit words. Both configurations require three standard 8-1/2 inch wide modules: two are hex-height and one is quad-height.

The quad-height module contains the memory stack: module H213 for 4K; and module H214 for 8K. One hex-height module (G110) contains the control logic, inhibit drivers, sense amplifiers, and 16-bit data register; the other hex-height module (G231) contains the address selection logic, current generator, and switches and drivers. Pin-to-pin compatibility exists between the C, D, E, and F connectors of both these modules are also compatible with the standard Unibus pin assignments.

It is recommended that the G231 Driver Module be installed between the G110 Control Module and the H213 or H214 Stack Module. Photographs of the component sides of the modules are shown in Figures 11-1, 11-2, and 11-3.

11.2.2 Specifications

The general memory specifications are listed in Table 11-1.

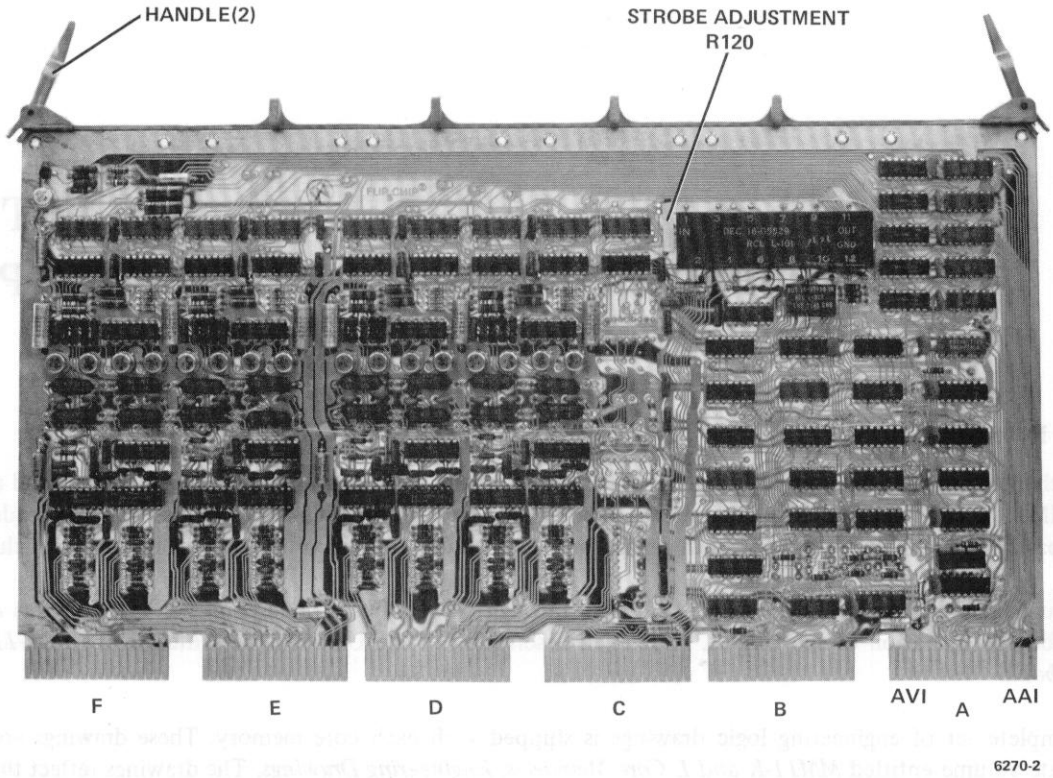


Figure 11-1 Component Side of G110 Control Module

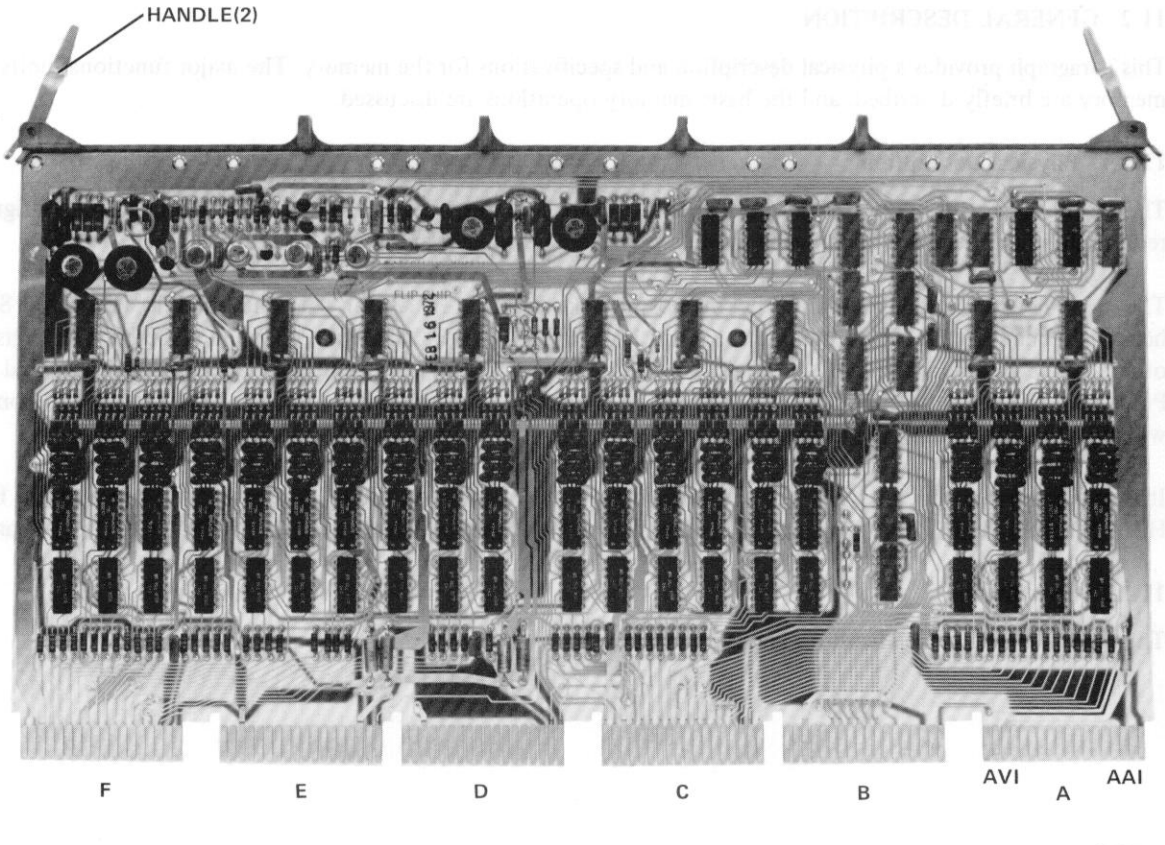


Figure 11-2 Component Side of G231 Driver Module

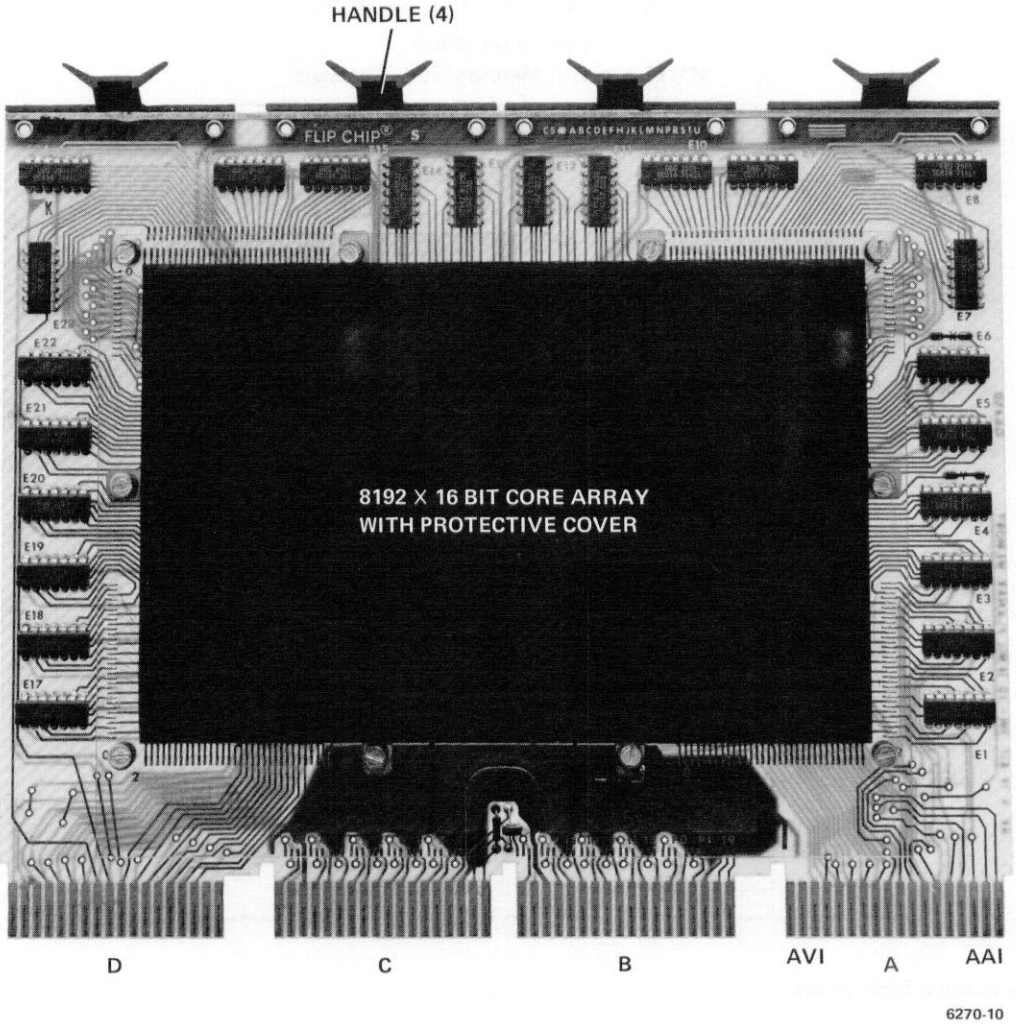


Figure 11-3 Component Side of 8K H214 Stack Module

Table 11-1
MM11-K and L Memory Specifications

Type:
Magnetic core, read/write, coincident current, random access.

Organization:
Planar, 3D, 3-wire

Capacity:
4096 (4K) words for MM11-K
8192 (8K) words for MM11-L

Access Time and Cycle Time:

Bus Mode	Cycle Time	Access Time
DATI	900 ns	400 ns
DATIP	450 ns	400 ns
DATO DATOB (PAUSE L)	900 ns	200 ns
DATO-DATOB (PAUSE H)	450 ns	200 ns

Table 11-1 (Cont)
MM11-K and L Memory Specifications

X-Y Current Margins:
±6% @ 0° C, ±7% @ 25° C, ±6% @ 50° C

Strobe Pulse Margins:
±30 ns @ 0° C, ±40 ns @ 25° C, ±30 ns @ 50° C

Voltage Requirements:
+5V ±5% with less than 0.05V ripple
-15V ±5% with less than 0.05V ripple

Average Current Requirements:
Stand by
+5V: 1.7A
-15V: 0.5A
Memory Active
+5V: 3.4A
-15V: 6.0A

Power Dissipation (worst case):
Control Module (G110): ≅ 60W
Drive Module (G231): ≅ 40W
Stack Module (H213 or H214): ≅ 20W
Total at maximum repetition rate: 120W

Environment:
Ambient temperature: 0° C to 50° C (32° F to 122° F)
Relative Humidity: 0–90% (non-condensing)

11.2.3 Functional Description

The memory is a read/write, random access, coincident current, magnetic core type with a cycle time of 900 ns and an access time of 400 ns. It is organized in a 3D, 3-wire planar configuration. Word length is 16 bits, and the memory is offered in two word capacities: the MM11-K contains 4096 (4K) words, and MM11-L contains 8192 (8K) words. The major functional units of the memory (Figure 11-4) are briefly described in the following paragraphs.

11.2.3.1 G110 Control Module – The G110 Control Module contains the memory control circuits, inhibit drivers, sense amplifiers, data register, threshold circuit, -5V supply, and device selector.

a. *Memory Control Circuits* – Control circuits are provided to acknowledge the request of the master device, determine which of the four basic operations (DATI, DATIP, DATO or DATOB) is to be performed, and set up the appropriate timing and control logic to perform the desired read or write operation. If a byte operation has been selected, address line A00 L determines the byte to be selected. The actual read or write operation is selected by control lines (C00 and C01). The memory control logic also transfers data to and from the Unibus.

b. *Inhibit Driver* – Each bit mat contains a single inhibit/sense line that passes through all cores on the mat. To write a 0 into a selected bit, an inhibit current is passed through the inhibit/sense line that cancels the write current in the Y-line. The core does not switch, so it remains in the 0 state. With no inhibit current, the currents in the X- and Y-lines switch the core to the 1 state.

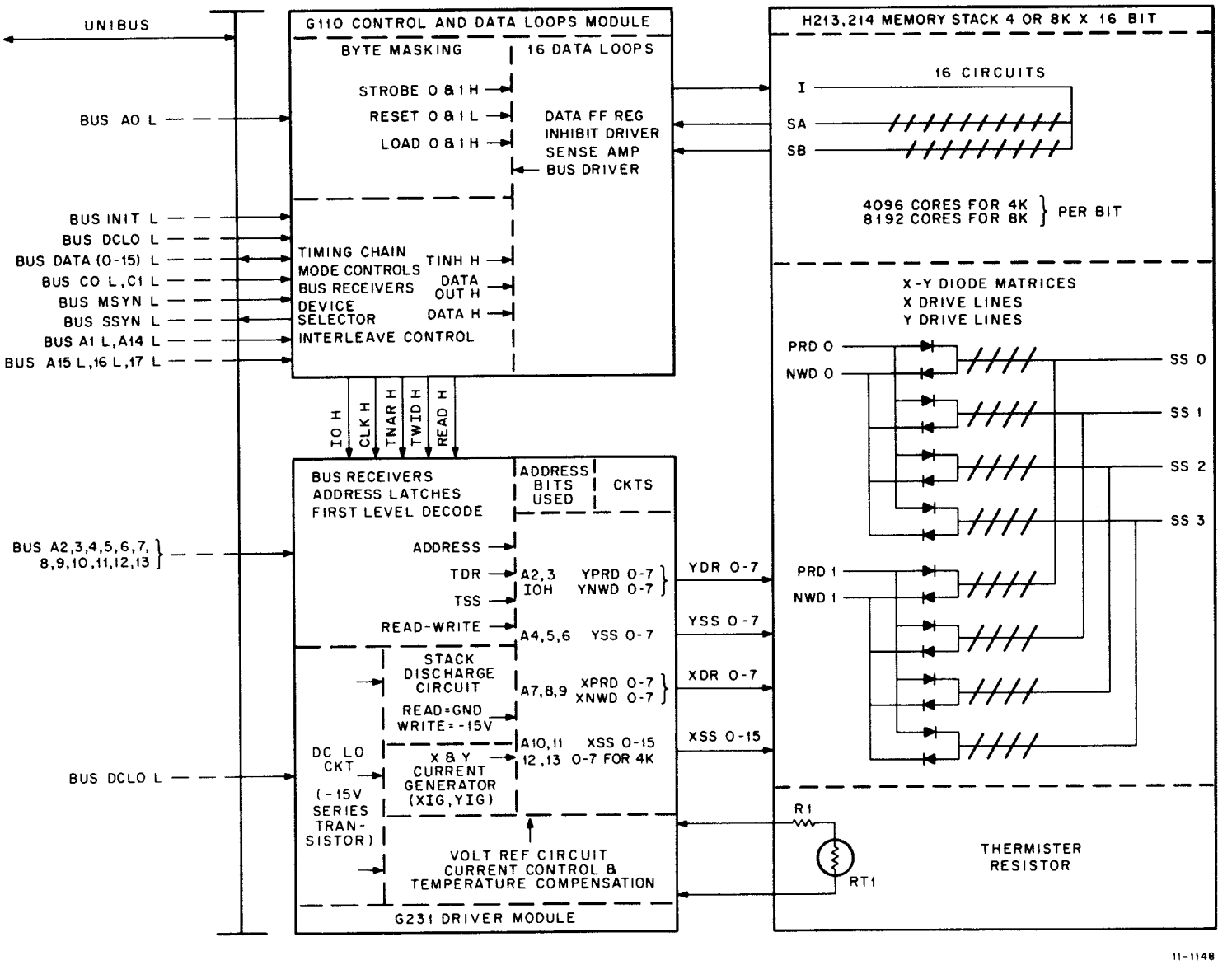


Figure 11-4 MM11-K, L Memory Block Diagram

c. *Sense Amplifiers* – During a read operation, the sense amplifier picks up a voltage induced in the sense/inhibit winding when a core is switched from a 1 to a 0. This signal is detected and amplified by the sense amplifier whose output sets a data register flip-flop to store a 1. In effect, a 1 is read but the core is switched to the 0 state. Cores which were previously set to 0 are not effected.

d. *Data Register* – The data register is a 16-bit flip-flop register used to store the contents of a word after it is destructively read out of the memory; the same word can then be written back into memory (restored) when in the DATI mode. The register is also used to accept data from the Unibus lines to accommodate the loading of incoming data into the core memory during the DATO or DATOB cycles.

e. *Device Selector* – The device address is decoded in the device selector to determine if the memory bank has been addressed.

f. *Threshold Circuit and -5V Supply* – The threshold circuit provides a reference threshold voltage to the sense amplifiers. During a read operation, if the threshold voltage (20 mV) is exceeded, the sense amplifier produces an output. The -5V supply provides a negative voltage for the sense amplifiers.

11.2.3.2 G231 Driver Module – The G231 Driver Module contains the address selection logic, switches and drivers, current generator, stack discharge circuit, and DC LO protection circuit.

a. *Address Selection Logic* – The core memory receives an 18-bit address from the master device. The address is latched and decoded to determine if the memory is the selected device and to determine the core location specifically addressed. If the operation is a byte operation, bus line A00 L indicates the byte to be used. The X- and Y-portion of the address is decoded through selection switches and a diode matrix to enable passage of read/write current through the selected X- and Y-drive lines of the memory. The coincidence of these currents selects the specific 16-bit core memory location desired.

b. *Switches and Drivers* – The switches and drivers direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because a single read/write line is used, and the current for a write operation is opposite in polarity to the current required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

c. *Current Generators* – X- and Y-current generators provides the current necessary to change the state of the magnetic cores. The linear rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

d. *Stack Discharge Circuit* – The stack discharge circuit maintains the proper stack charge voltage during operation: approximately 0V during a read operation and approximately -14V during a write operation.

e. *DC LO Protection Circuit* – If any dc voltage is out of tolerance, DC LO is asserted on the Unibus. It is sensed by the DC LO protection circuit, which inhibits the memory operation by opening the -15V line to the current source. This prevents spurious memory operation.

11.2.3.3 H213 or H214 Stack Module – The stack module contains the ferrite core array and the X-Y diode matrices. For the 4K memory (H213), 16 core mats are used, each wired in a 64 X 64 matrix; 16 core mats, each wired in a 128 X 64 matrix are used for the 8K memory (H214). The stack also contains the resistor/thermistor combination to control the X-Y current generator temperature compensation.

11.2.4 Basic Memory Operations

The core memory has four basic modes of operation. The main function of the memory is simply to read and write data. Additional modes are provided, however, to allow for byte operation and to eliminate the restore cycle when it is not needed, thereby increasing overall system efficiency. The four basic memory operations are:

a. Read/restore (DATI)
b. Read pause (DATIP)
c. Write (DATO)
d. Write byte (DATOB).

These four modes are discussed briefly in the following paragraphs.

NOTE

In the following discussions, all operations refer to the master (controlling) device. For example, the term "data out" indicates data flowing out of the master and into the memory.

11.2.4.1 Data In (DATI) Cycle – The DATI cycle is a read/restore memory cycle. During this operation, the memory reads the information from the selected core location, transfers it to the Unibus, and then writes the information back into the memory location. This last step is necessary because the core memory is a destructive readout device. During the first part of the cycle, the memory loads the data into a register; at the same time, the memory applies the data to the Unibus. Then, during the second part of the cycle, the memory takes the data from the register and writes it back into the addressed memory location.

11.2.4.2 Data In, Pause (DATIP) Cycle – Normally in reading from memory, the information is destroyed in the particular location accessed, and the data must be restored. However, sometimes it is not actually necessary to restore the information after reading, because the location is to have new data written into it. In this instance, eliminating the restore operation decreases the memory cycle time by approximately 50 percent. The DATIP operation is used for this purpose. The data is read from memory and the restore cycle is inhibited. Because no restore cycle is used, a DATIP must always be followed by a write cycle (either DATO or DATOB) on the same address or data in both addresses will be destroyed. If a DATIP is not followed by a DATO or DATOB, the memory controller will be unable to control the bus, and other devices will be unable to access the bus (this is known as hanging the bus).

11.2.4.3 Data Out (DATO) Cycle – The DATO cycle is a write memory cycle used by the master device to transfer data into core memory. To ensure that proper data is stored, the memory unit must first be cleared by reading the cores (thereby setting them all to 0) before writing in the new data. During a normal DATO, the memory first performs the read operation to clear the cores and then performs a write cycle to transfer data from the bus into the selected core location. If a DATO follows a DATIP (rather than a DATI), the sequence is not the same. The DATIP clears core and generates a pause flag; the DATO skips the read cycle and immediately begins the write cycle. This process reduces DATO cycle time by approximately 50 percent.

11.2.4.4 Data Out, Byte (DATOB) Cycle – The DATOB cycle is similar in function to the DATO cycle, except that during DATOB data is transferred into the core memory from the bus in byte form rather than as a full word. During the read cycle, the non-selected byte is saved by reading it into the data register while the selected byte is transferred into the register from the bus. During the write cycle, only the selected byte portion of the word is loaded into the memory location from the bus. At the same time, the non-selected byte is restored from the data register into the memory location. In effect, the memory is first cleared and then simultaneously performs a restore cycle for the non-selected byte and a write cycle for the selected byte. This mode can follow a DATIP as described above.

CHAPTER 12
MM11-K AND L DETAILED DESCRIPTION

12.1 INTRODUCTION

This chapter provides a detailed description of the MM11-K and L memories. The discussion is related to the 8K memory (MM11-L). The description of the 4K memory (MM11-K) is basically the same; only the differences are discussed.

The detailed description covers the core array, device and word selection, switches and drivers, current generation, stack discharge circuit, DC LO circuit, sense/inhibit circuitry, control and timing logic, and memory operating cycles.

12.2 CORE ARRAY

The ferrite-core array for the 8K memory consists of 16 mats arranged in a planar configuration. Each mat contains 8192 ferrite cores arranged in a 128 X 64 array. Each mat represents a single bit position of a word. This planar configuration provides a total of 8192 16-bit word locations. The 4K memory core array consists of 16 mats each arranged in a 64 X 64 planar configuration to provide a total of 4096 16-bit word locations. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or a binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals. The outside diameter of each core is 18 mil; the inside diameter is approximately 11 mil. Each core is 4.5 mil thick.

Selection and switching of the cores is provided by three wires traversing each core in a special selection technique. An X-axis read/write winding passes through all cores in each horizontal row for all 16 mats. A Y-axis read/write winding passes through all cores in each vertical row for all 16 mats. Through the use of selection circuits which control the current applied to specific X-Y windings, any one of the 8192 or 4096 word locations can be addressed for writing data into memory or reading data out of memory. A third line passes through each core on a mat to provide the sense/inhibit functions. There is one sense/inhibit line per mat. This single sense/inhibit line, as well as the selection circuits, are discussed in subsequent paragraphs.

12.3 MEMORY OPERATION

Figure 12-1 illustrates a typical portion of the core memory. An X- and Y-winding pass through each core in the mat. The current passing through any one winding is such that no single winding produces a magnetic field strong enough to cause a core to change its magnetic state. Only the reinforcing magnetic field caused by the coincident current of both an X- and Y-winding can cause the core located at the point of intersection to change states. It is this principle that allows the relatively simple winding arrangement to select one and only one memory core out of the total contained on each mat. The current passing through either an X- or Y-winding is referred to as the half-select current.

A half-select current passing through the X3 winding (Figure 12-1) from left to right produces a magnetic field that tends to change all cores in that horizontal row from the 0 to 1 state. The flux produced by the current is, however, insufficient to complete the state transition in any core. Simultaneously passing a half-select current through the Y2 winding from top to bottom produces the same effect on all cores in that particular vertical row. Note, however, that both currents pass through only one core which is located at the intersection of the X3 and Y2 windings. This is

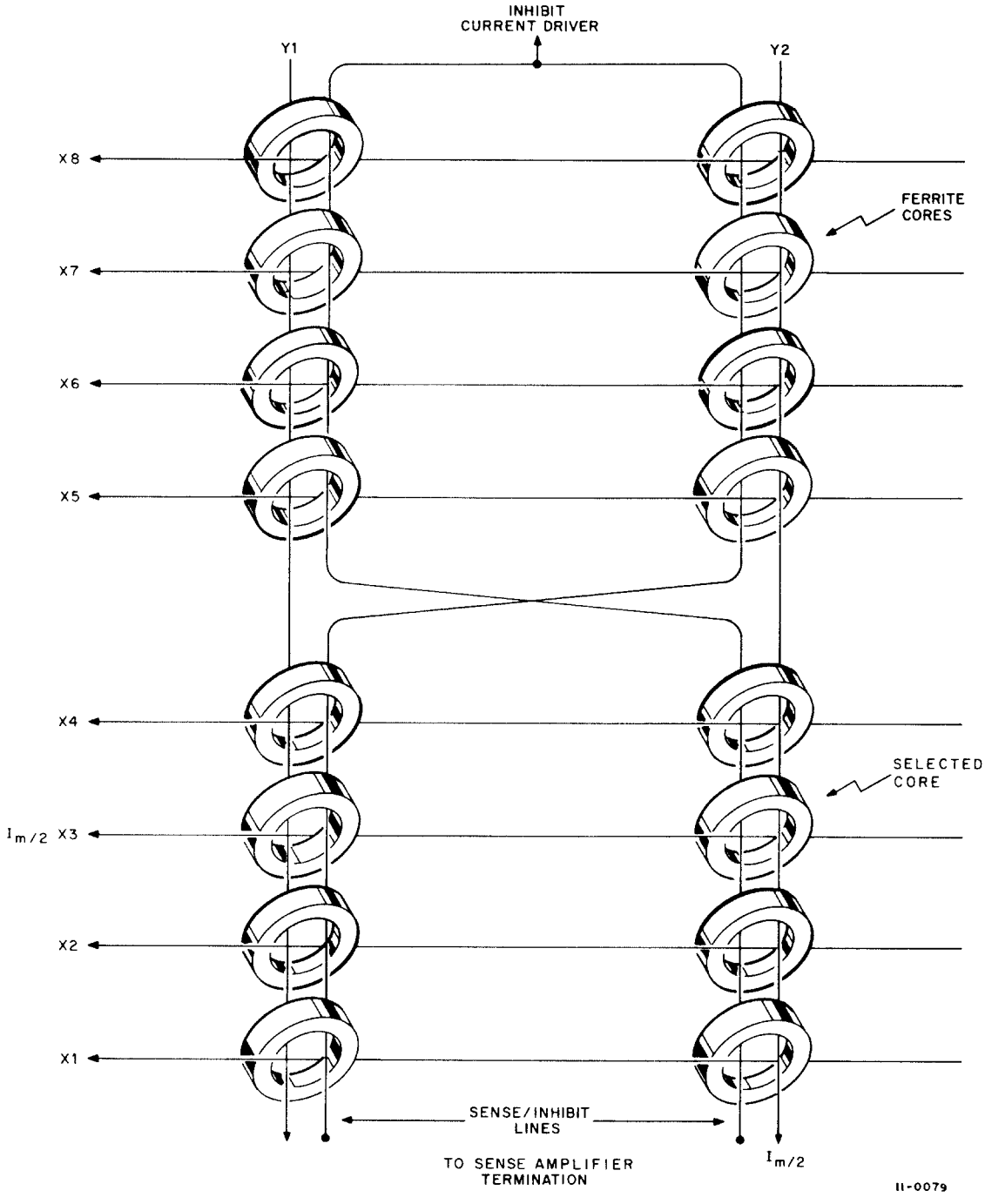


Figure 12-1 Three-Wire Memory Configuration

the selected core and the combined current values are sufficient to change the state of the core. The arrows in Figure 12-1 show current direction for the write cycle. All X- and Y-windings are arranged in such a manner that whenever a half-select current is passed through each, the resultant magnetic fields combine in the core at the point of intersection. This combined, full-select current ensures that the selected core is left in the binary 1 state. The currents used to select the core are referred to as write currents. A typical hystersis loop for a core is shown in Figure 12-2.

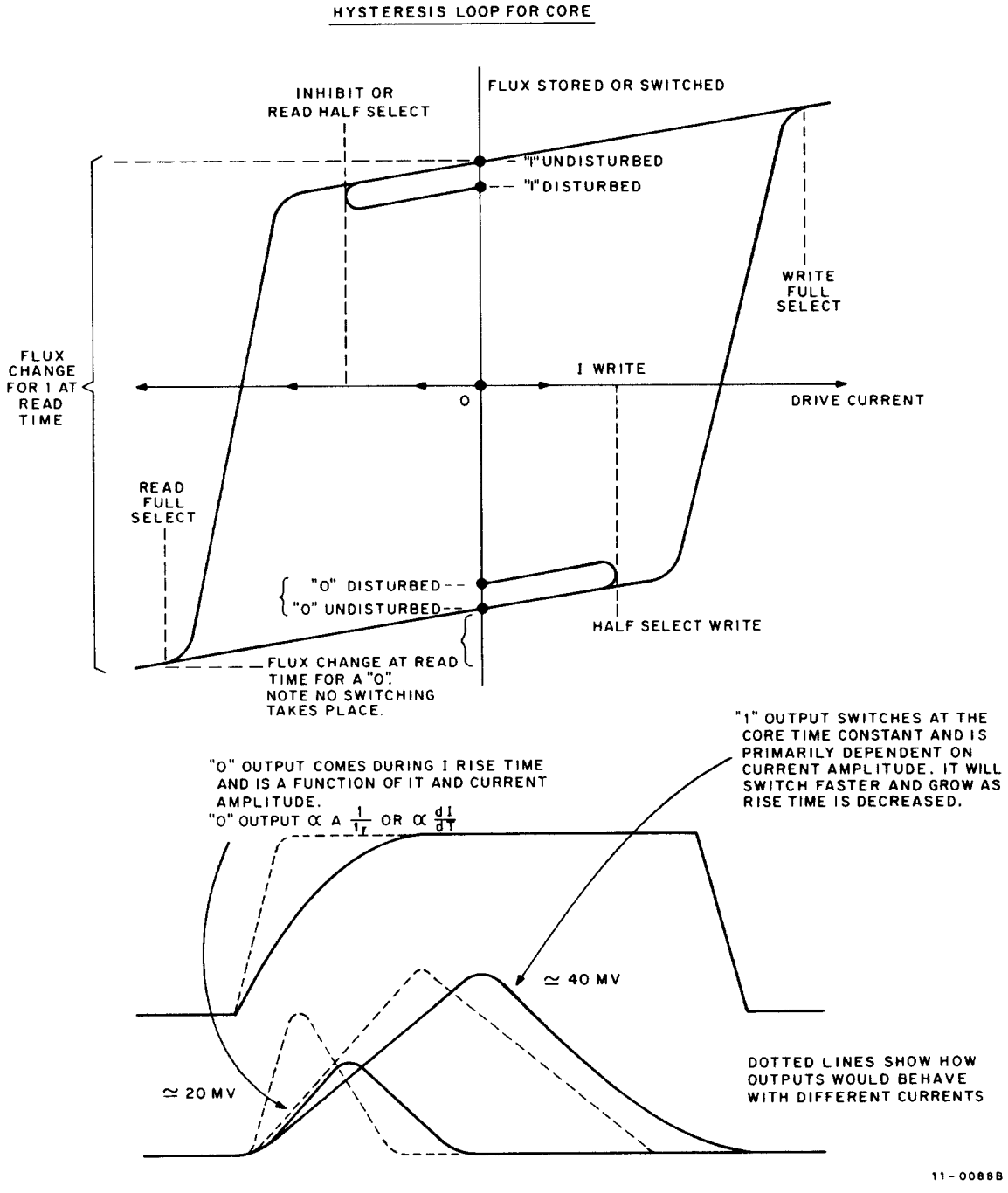


Figure 12-2 Hysteresis Loop for Core

In the MM11-K and L Core Memories, the X3 windings in all 16 mats are connected in series as are the Y2 windings. Therefore, whenever a full-select current flows through a selected core on one mat, it also flows through an identical core on the other 15 mats. The X3-Y2 cores on all mats switch to a binary 1, causing each of the 16 cores to become one bit of a 16-bit storage cell.

Because of the serial nature of the X-Y windings, a method is used that allows cores to remain in the 0 state during a write operation; otherwise, every 16-bit word selected would be all 1s. The method used in the MM11-K and L Core Memories is to first clear all cores to the 0 state by reading and then, by using an inhibit winding during the write operation, to inhibit cores on particular mats. The inhibited cores remain 0s even when identical cores on other mats are set to 1.

The half-select current for the inhibit lines is applied from an inhibit current driver, which is a switch and a resistor between the inhibit line and -15V. The current in the inhibit line flows in the opposite direction from the write current in all Y-lines and cancels out the write current in any Y-line. There is a separate inhibit driver for each memory mat, and each mat represents one bit position of a word; thus, selected bits can be inhibited to produce any combination of binary 1s and 0s desired in the 16-bit word. It must be remembered that the inhibit function is active only during write time.

The sense/inhibit lines are also used to read out information in a selected 16-bit memory cell. The specific core is selected at read time in the same manner as during the write cycle with one notable exception: the X- and Y-currents are in the opposite direction. These opposite half-select currents cause all cores previously set to 1 to change to 0; cores previously set to 0 are not effected. Whenever the core changes from 1 to 0, the flux change induces a current in the sense winding of that mat. This current is detected and amplified by a sense amplifier. The amplifier output is strobed into the data register for eventual transfer to the Unibus. Figure 12-3 shows a 16-word by 4-bit planar memory. The MM11-L Core Memory (8K) functions in the same manner, except that it has 128 X-lines, 64 Y-lines, and 16 core mats. The core stringing is identical, and the sense windings are strung through all 8192 cores with the interchange between X63 and X64 instead of between X1 and X2. For the 4K memory, the interchange is between X31 and X32 and it has 64 X-lines and 64 Y-lines.

12.4 DEVICE AND WORD SELECTION

When the processor or a peripheral device attempts to perform a transaction with the memory, the processor asserts an 18-bit address on Unibus address lines A (17:00). Six of these 18 bits [A01 and A (17:13)] indicate the address of the memory as a device. Depending on the memory configuration, only four or five bit combinations of these bits are used as shown in Table 12-1. Eleven of the 12 remaining bits [A (12:02)] plus A01 and A13 indicate the address of a specific word within the memory. Address bit A00 is used to select the byte (8 bits) transaction when in DATOB mode.

Table 12-1
Addressing Functions

Bus Address	Function	
	4K Mode	8K Mode
A00	Controls byte mode	Controls byte mode
A01	Becomes A01H to G231	Becomes A01H to G231
A02, A03, A01H*	Decode Y-Drivers	Decode Y-Drivers
A04, A05, A06	Decode Y-Switches	Decode Y-Switches
A07, A08, A09	Decode X-Drivers	Decode X-Drivers
A10, A11, A12	Decode X-Switches	Decode X-Switches
A13	Goes to device selector	Decode X-Switches
A14	Goes to device selector	Goes to device selector
A15, A16, A17	Goes to device selector	Goes to device selector

*A01H is not a Unibus signal.

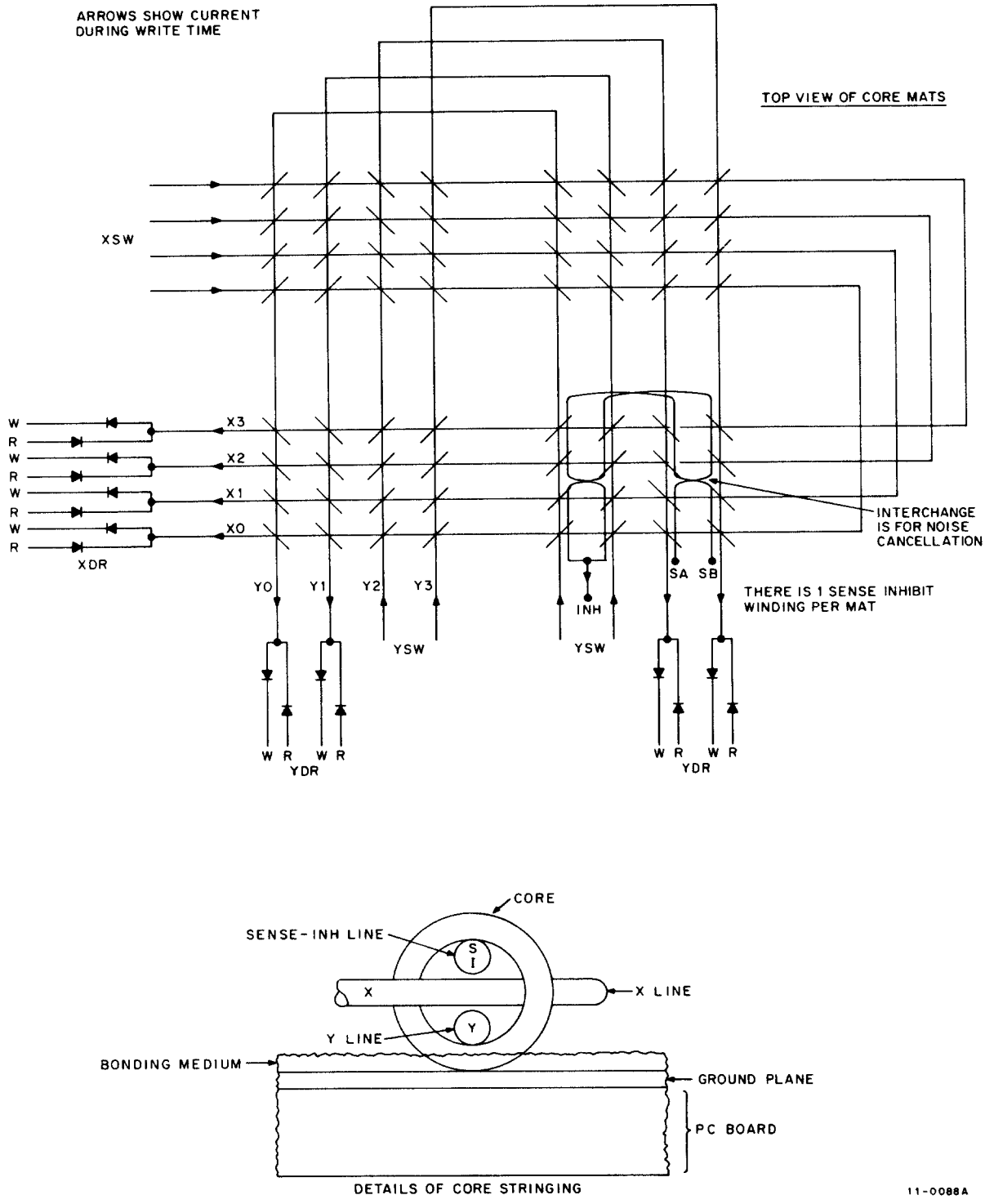


Figure 12-3 Three-Wire 3D Memory, Four Mats Shown for a 16-Word 4-Bit Memory

The memory address is decoded by the device selection circuit on the G110 Control Module. The word address is stored in a register on the G231 Driver Module whose output is decoded to activate the X-Y line switches and drivers which select the addressed word. These circuits contain jumpers which are included or excluded to establish a specific device address and select 4K- or 8K-word capacity. Jumpers are provided to select interleaved or non-interleaved operation for the 8K model; however, the memory is to be operated in the non-interleaved mode only.

Table 12-1 lists the function of each address bit. Figure 12-4 is a simplified block diagram of the device and word address selection circuits.

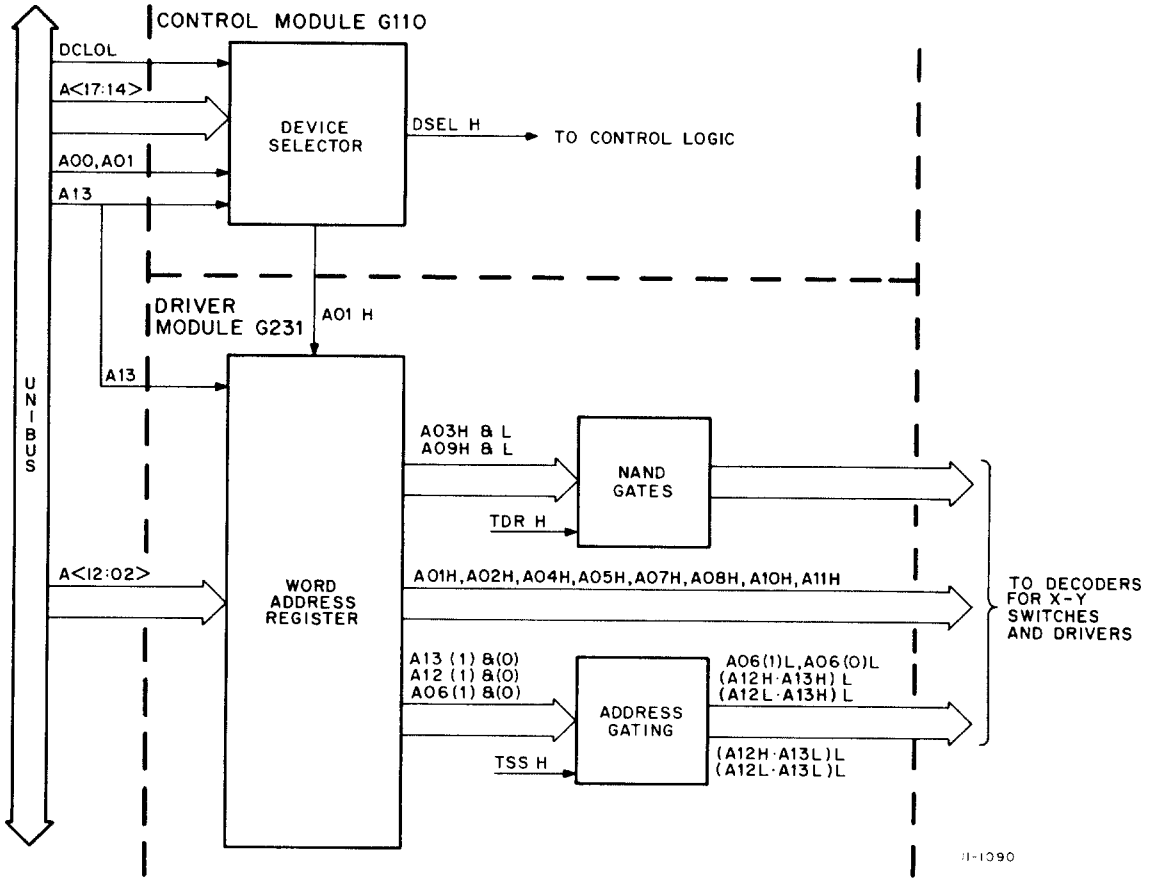
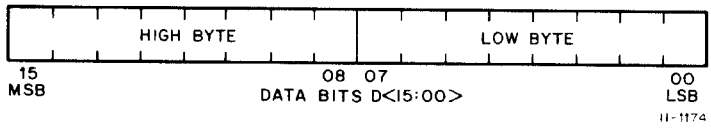


Figure 12-4 Device and Word Address Selection Logic, Block Diagram

12.4.1 Memory Organization and Addressing Conventions

Prior to a detailed discussion of the address selection logic, it is important to understand memory organization and addressing conventions.

The memory is organized in 16-bit words each consisting of two 8-bit bytes. The bytes are identified as low and high as shown below.



Each byte is addressable and has its own address location: low bytes are even numbered and high bytes are odd numbered. Words are addressed at even numbered locations only; the high (odd) byte is automatically included.

For example, an 8K word memory has 8192 words or 16,384 bytes; therefore, 16,384 locations are assigned. The address locations are specified as 6-digit octal numbers. The 16,384 locations for the 8K memory are designated 000000 through 037777. Figure 12-5 shows the organization for an 8K memory.

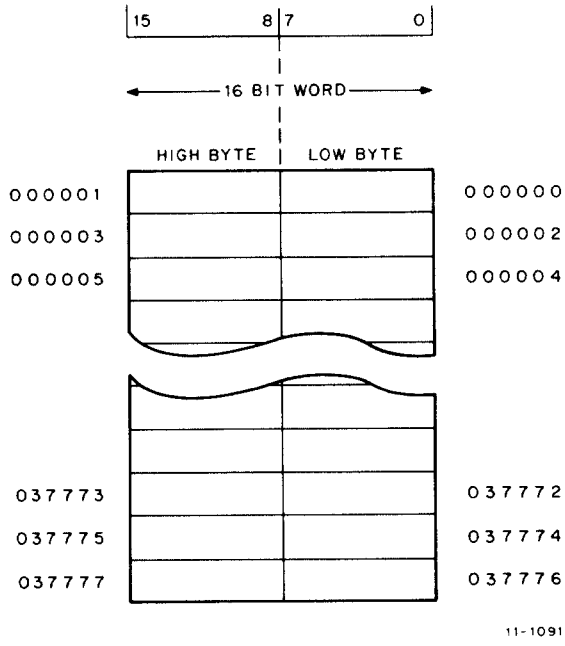


Figure 12-5 Memory Organization for 8K Words

The address selection logic responds to the binary equivalent of the octal address. The binary equivalent of 017772 is shown in the following example.

ADDRESS BITS A<17:00>

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT POSITION
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	BINARY
0			1			7			7			7			2			OCTAL

11-1173

Each memory bank (4K or 8K words) requires its own unique device address. For example, assume that a system contains three 8K memory banks (Figure 12-6). The device selector for the 8K non-interleaved memory decodes four address lines [A (17:14)]. Examination of the binary states of these bits for the three memory banks shows that the changes in the states of bits A14 and A15 allow the selection of a unique combination for each bank. The combination, which is the device address, is hardware-selected by jumpers in the device selector.

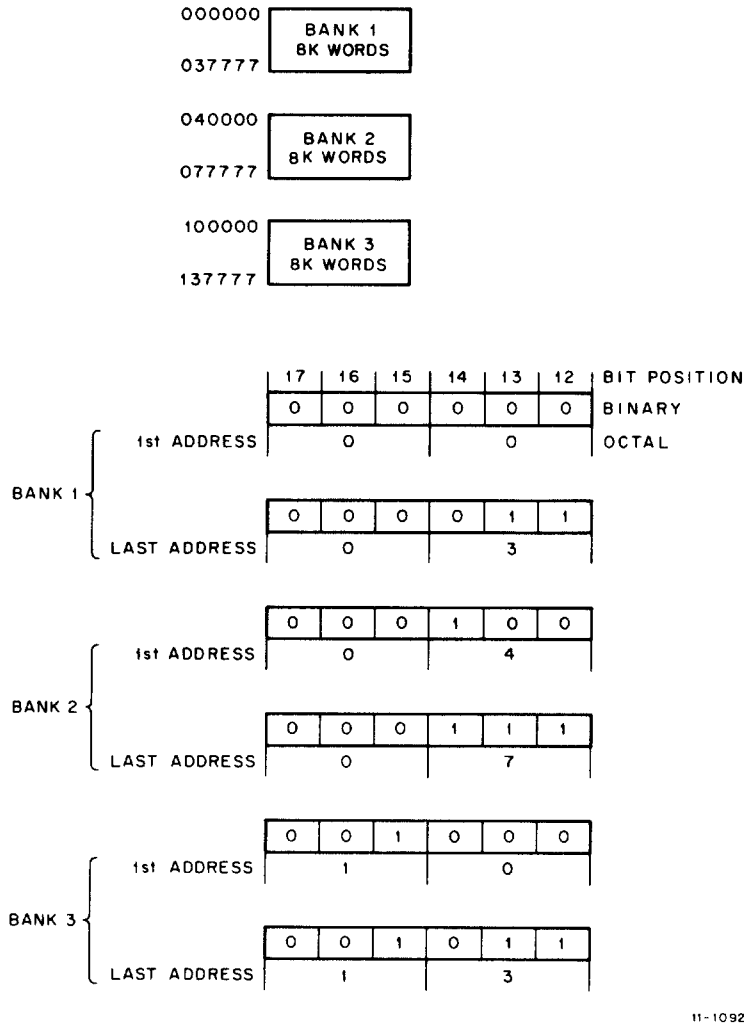


Figure 12-6 Address Assignments For Three Banks of 8K Words Each

During system operation, the processor generates the binary equivalent of the octal address on Unibus address lines A (17:00). The processor uses positive logic and the Unibus uses negative logic. With this in mind, the following is included to remind the reader of the negative logic convention of the Unibus.

Processor (Positive Logic)
Signal Asserted: High = Logical 1 = +3V
Signal at Rest: Low = Logical 0 = 0V

Unibus (Negative Logic)
Signal Asserted: Low = Logical 1 = 0V
Signal at Rest: High = Logical 0 = +3V

12.4.2 Device Selector

The device selector located on the G110 Control Module (drawing G110-0-1, sheet 2) shows a logic diagram of the device selector in the 4K configuration.

Address bits A01 and A (17:13) are decoded in the device selector to provide the device selection signal D SEL H that is used in the control logic. Two combinations of these bits are decoded, depending on the memory configuration as shown below.

Memory Configuration	Address Bits
4K Words	A (17:13)
8K Words	A (17:14)

Obviously, the memory capacity is determined by the stack module: H213 for 4K words and H214 for 8K words. The same control module is used for both 4K and 8K memories; therefore, two jumpers (W9 and W10) are provided to include or exclude address bit A13 commensurate with the memory word size. Two jumpers (J3 and J4) on the G231 Driver Module (drawing G231-0-1, sheet 2) are provided for A13 inclusion or exclusion in the word addressing logic. The same driver module is used for both memory capacities. In the 4K word size, the components associated with the additional X-line read and write switches needed for 8K words may be removed. Two jumpers (W7 and W8) in the device selection logic on the control module are used to select interleaved or non-interleaved operation of the 8K memory. They are configured to provide non-interleaved operation only.

Each memory bank (4K or 8K) must have its own unique device address. Five jumpers (W2-W6) in the device selector provide this capability. On drawing G110-0-1, sheet 2, all the jumpers are shown in place and the device selector responds only when high signals appear on the Unibus address lines A (17:13). Some jumpers can be removed to allow the device selector to respond to a particular combination of high and low signals on these address lines.

All highs at the inputs of the 7380 Unibus receivers (E12 and E23) give lows at their outputs. Each receiver output goes to one input of a type 8242 Exclusive-NOR gate. Because of jumpers W7 and W8, bit A14 is decoded for 4K and 8K configurations. An additional receiver is used to sense BUS DC LO L, and its output (E23 pin 14) is sent to an 8242 gate (E24 pin 5). BUS DC LO L is asserted only when the dc voltages from the power supply drop below specified limits.

The other input of the 8242 gates associated with bits A14, A13, A15, A16 and A17 can be connected to +5V or ground, depending on whether or not jumpers W2-W6 are installed. The input is low (ground) with the jumper in; with the jumper removed, the input is high (+5V). Each 8242 gate is used as a digital comparator; its output is high only when both inputs are identical. The 8242 gates have open collectors and they are connected in common; therefore, the comparator output D SEL H is high only when all gates detect matched inputs (both lows or both highs).

An installed jumper requires a low signal at the output of the 7380 Unibus receiver. The 7380 is connected as an inverter so this signal is reflected as a high on the Unibus (logical or asserted state for the Unibus). To configure the jumpers for a specific device address, find the binary equivalent of the assigned octal address and insert a jumper in each bit position that contains a 0. A specific jumper configuration is shown in Figure 12-7.

The previous discussion dealt with the 4K memory configuration of the device selector as shown in drawing G110-0-1, sheet 2. Address bits A (17:13) are decoded and the output of bit A01 Unibus receiver (E23 pin 2) is sent via jumper W8 to the word address register as A01 H.

In the 8K memory configuration, jumper W9 is removed and W10 is installed. This removes bit A13 from the input of Unibus receiver E12 on G110 and replaces it with +5V via resistor R107. This receiver output (pin 14) always remains low so that jumper W5 must remain installed to ensure a match on pins 12 and 13 of gate E13. The jumper configurations for memory systems up to 128K words are shown in Figure 12-8.

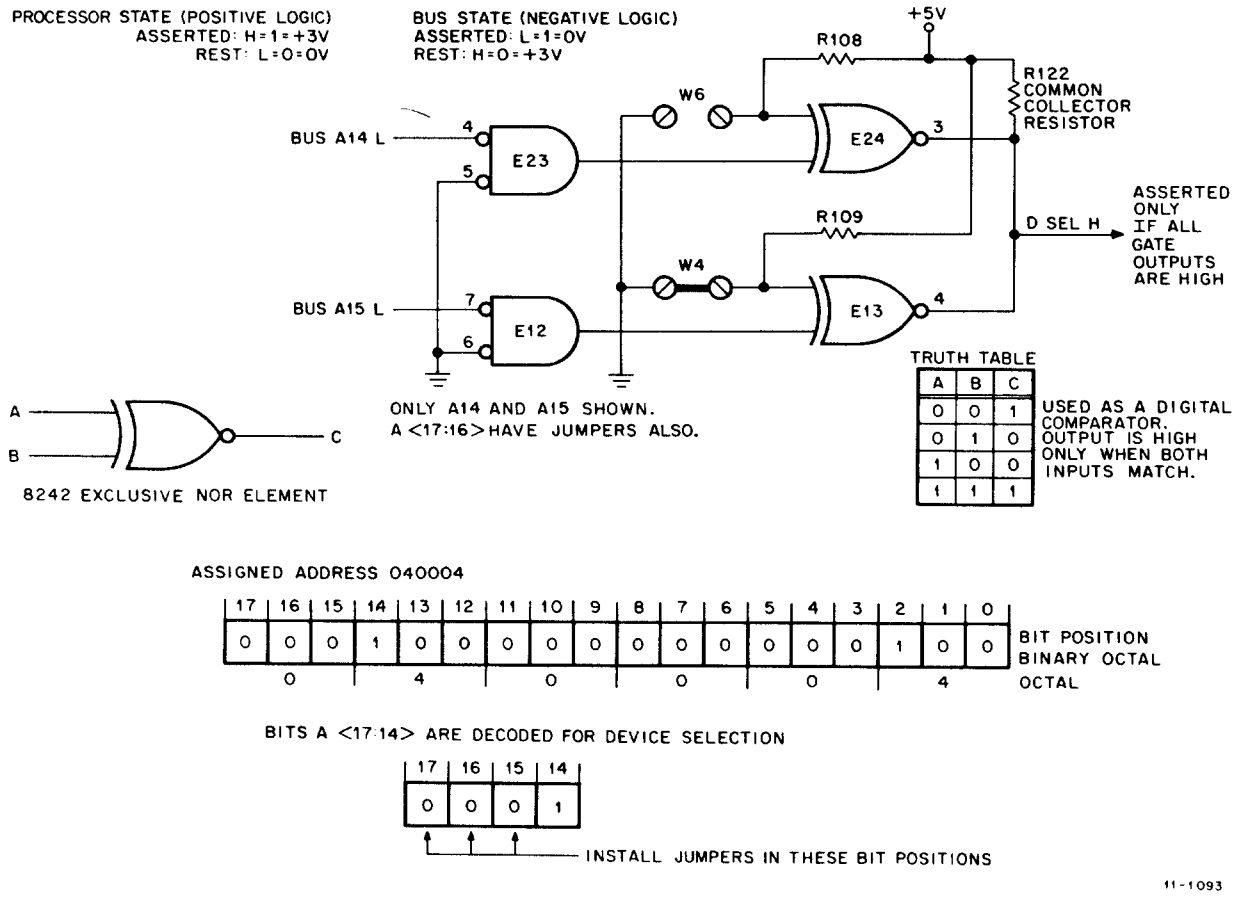
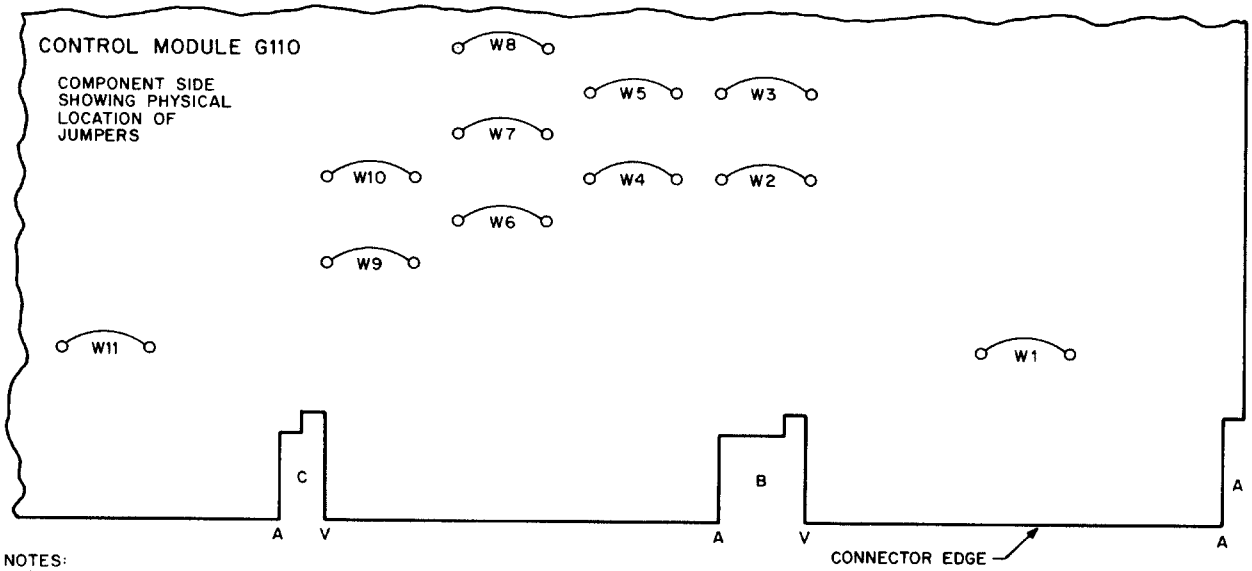


Figure 12-7 Jumper Configuration For A Specific Memory Address



NOTES:
1. Jumper W1 is for test purposes only. It must be installed for normal operation.
2. Jumper W11 should be removed for normal operation. When installed the memory responds to DATI only, regardless of state of control lines C00 and C01.
3. Jumpers W7 and W8 must remain in the factory installed positions.
4. When used as an 8k bank, jumpers W5 and W10 must be installed and jumper W9 must be removed.
5. When used as a 4k bank, jumper W10 must be removed and jumper W9 must be installed. Jumper W5 determines the location of the bank on the bus.

Figure 12-8 Device Decoding Guide

Memory Bank (Words)	Machine Address (Words)	Device Address Jumpers				
		W5 A13	W6 A14 or A01	W4 A15	W3 A16	W2 A17L
0–4K	000000–017776	IN	IN	IN	IN	IN
4–8K	020000–037776	OUT	IN	IN	IN	IN
8–12K	040000–057776	IN	OUT	IN	IN	IN
12–16K	060000–077776	OUT	OUT	IN	IN	IN
16–20K	100000–117776	IN	IN	OUT	IN	IN
20–24K	120000–137776	OUT	IN	OUT	IN	IN
24–28K	140000–157776	IN	OUT	OUT	IN	IN
28–32K	160000–177776	OUT	OUT	OUT	IN	IN
32–36K	200000–217776	IN	IN	IN	OUT	IN
36–40K	220000–237776	OUT	IN	IN	OUT	IN
40–44K	240000–257776	IN	OUT	IN	OUT	IN
44–48K	260000–277776	OUT	OUT	IN	OUT	IN
48–52K	300000–317776	IN	IN	OUT	OUT	IN
52–56K	320000–337776	OUT	IN	OUT	OUT	IN
56–60K	340000–357776	IN	OUT	OUT	OUT	IN
60–64K	360000–377776	OUT	OUT	OUT	OUT	IN
64–68K	400000–417776	IN	IN	IN	IN	OUT
68–72K	420000–437776	OUT	IN	IN	IN	OUT
72–76K	440000–457776	IN	OUT	IN	IN	OUT
76–80K	460000–477776	OUT	OUT	IN	IN	OUT
80–84K	500000–517776	IN	IN	OUT	IN	OUT
84–88K	520000–537776	OUT	IN	OUT	IN	OUT
88–92K	540000–557776	IN	OUT	OUT	IN	OUT
92–96K	560000–577776	OUT	OUT	OUT	IN	OUT
96–100K	600000–617776	IN	IN	IN	OUT	OUT
100–104K	620000–637776	OUT	IN	IN	OUT	OUT
104–108K	640000–657776	IN	OUT	IN	OUT	OUT
108–112K	660000–677776	OUT	OUT	IN	OUT	OUT
112–116K	700000–717776	IN	IN	OUT	OUT	OUT
116–120K	720000–737776	OUT	IN	OUT	OUT	OUT
120–124K	740000–757776	IN	OUT	OUT	OUT	OUT
124–128K	760000–777776	OUT	OUT	OUT	OUT	OUT

Figure 12-8 Device Decoding Guide (Cont)

12.4.3 Word Selection

Word selection requires two levels of decoding. The word address bits are placed in the 13-bit word address register: 12 bits are used for a 4K memory, and 13 bits are used for an 8K memory. Some bits from the register output are combined in a gating network. The outputs from the gating network and some outputs directly from the register are used as inputs to a group of decoders (Figure 12-4). The outputs of the decoders select the proper X- and Y-read/write switches and drivers.

12.4.3.1 Word Address Register and Gating Logic – The word address register and gating logic are contained on the G231 Driver Module. The circuit schematic is shown in drawing G231-0-1, sheet 2. The register is composed of 13 74H74 dual D-type edge-triggered flip-flops. They are identified as E11, E12, E13, E14, E18, E19, and E20. The output (pin 3) of gate E9 provides a high signal on the preset input (pin 4 or pin 10) of each flip-flop, which prevents direct presetting of the flip-flop. Direct clearing of each flip-flop is prevented by a high signal on the clear input (pin 1 or pin 13) via the output (pin 2) of gate E9. The register cannot be directly cleared or preset; its output responds only to the signal at its data (D) input.

Address bits A (13:02) are picked off the Unibus via type 7380 receivers (E15, E16, and E17). The receiver outputs are sent to the corresponding flip-flop D-inputs. The input to the receiver associated with bit A13 has two sources: Unibus signal BUS A13 L via jumper J4, or +5V via jumper J3. These jumpers are associated with the memory word size. A 4K memory requires J3 in and J4 out; an 8K memory requires J4 in and J3 out. Because BUS A13 L is used on the G110 module as part of the device selector, this arrangement prevents loading BUS A13 L twice per memory bank.

The E11 flip-flop associated with bit A01 receives its input from the device selector (drawing G110-0-1, sheet 2). The input signal is A01 H, which is obtained from bit A01 Unibus receiver for both 4K and 8K memories.

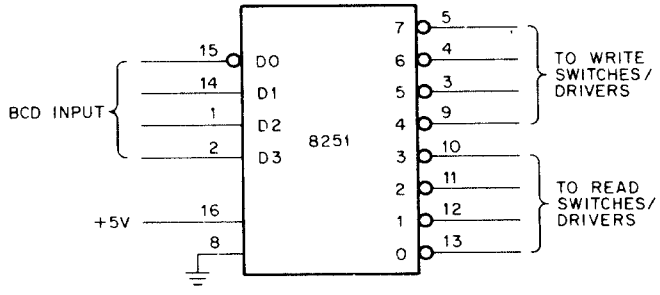
The register flip-flops are clocked synchronously by CLK 1 H from the control logic (drawing G110-0-1, sheet 2). Clocking occurs on the positive-going edge of CLK 1 H. The generation and timing of this clock signal is discussed in Paragraph 12.9.1. When the register is clocked, the outputs of flip-flops A01, A02, A04, A05, A07, A08, A10 and A11 are sent to the type 8251 X-Y decoders on the G231 Driver Module (drawing G231-0-1, sheets 3 and 4). The outputs of flip-flops A06, A12, and A13 are combined in a group of six type 74H10 NAND gates (three E22s, and three E25s), which are enabled by signal TSS H. Table 12-2 lists the states of flip-flops A06, A12, and A13 that are required to enable these gates. The outputs of flip-flops A03 and A09 are gated with TDR H in high-speed 2-input NAND gates and then applied to the decoders for the drivers only. The six signals listed in Table 12-2 are sent only to the X-Y line read/write switch decoders on the driver module.

Table 12-2
Enabling Signals for Word Register Gating

Output Signals		Enabling Signals		
Gate	Asserted Signal	FF A06	FF A12	FF A13
E22 pin 12	(A06H) L	Set	X	X
E22 pin 8	A06L	Reset	X	X
E22 pin 6	(A12H · A13H) L	X	Set	Set
E25 pin 12	(A12L · A13H) L	X	Reset	Set
E25 pin 8	(A12H · A13L) L	X	Set	Reset
E25 pin 6	(A12L · A13L) L	X	Reset	Reset

Signal ISS H is generated at the output (pin 3) of negative input OR gate E4 during a read or write operation. During a read operation, the enabling signal is produced at NAND gate E4, pin 8 by ANDing READ H and TNAR H. During a write operation, the enabling signal is produced at NAND gate E4, pin 6 by ANDing WRITE H and TWID H. Signals READ, TNAR and TWID are generated by the control logic on the G110 Control Module. WRITE is the complement of READ (produced by inverter E6). Signal READ H comes from the 1 output of R/W flip-flop E13 (drawing G110-0-1, sheet 2); the READ H signal is produced when the flip-flop is set. When the R/W flip-flop is cleared, READ H is low and is inverted by E6 to produce WRITE H.

12.4.3.2 X- and Y- Line Decoding – The basic decoding unit is a Type 8251 BCD-to-Decimal Decoder that converts a 4-bit BCD input code to a one-of-ten output; however, only eight outputs are used. Figure 12-9 shows an 8251 and associated truth table. The inputs are D0, D1, D2, and D3; they are weighted 1, 2, 4, and 8 with D0 being the least significant bit. The outputs are 0–7 and are mutually exclusive. The selected output is low and all others are high.



TRUTH TABLE

INPUTS				OUTPUTS							
D3	D2	D1	D0	0	1	2	3	4	5	6	7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	X	X	X	1	1	1	1	1	1	1	1

X = IRREVELANT

11-1095

Figure 12-9 Type 8251 Decoder, Pin Designation and Truth Table

For the 8K memory, ten decoders are used: six for the X-axis and four for the Y-axis. Each decoder controls four read/write switch pairs. Each pair is associated with a specific switch or driver. This switch matrix is combined with the stack X-Y diode matrix to allow selection of any location out of the total 8192 locations (stack drawing DCS-H214-0-1 for interconnections).

For the 4K memory, eight decoders are used, four for each axis. The stack X-diode matrix is halved to allow selection of any location out of the total 4096 locations (stack drawing DCS-H213-0-1 for interconnections). A discussion of the configuration and operation of the switches and diode matrices is given in Paragraph 12.4.3.3.

The X- and Y-line switches are first differentiated as switches and drivers. The drivers are those switches that are connected to the diode end of the stack. Drivers and switches are further differentiated by function: either read or write. Another differentiation is made by polarity: negative or positive, depending on the physical connection. Read drivers and write switches are connected to the current generator outputs and are considered positive; write drivers and read switches are connected to -15V and are considered negative.

Figure 12-10 shows the decoders associated with Y-line read and write switches 4–7 and Y-line read and write drivers 4–7. (Refer also to the truth table in Figure 12-9.) In both decoders (E28 for switches and E8 for drivers), the signal to input D3 selects the block of switch pairs. This signal must be low for any output to be selected. The signal to input D2, which is READ L for all decoders, controls the selection of read or write switches/drivers. When

READ L is low, outputs 0–3 are selected: these are read switches and read drivers. When READ L is high, outputs 4–7 are selected: these are write switches and write drivers. The four combinations of the states of inputs D0 and D1 select the particular switch/driver.

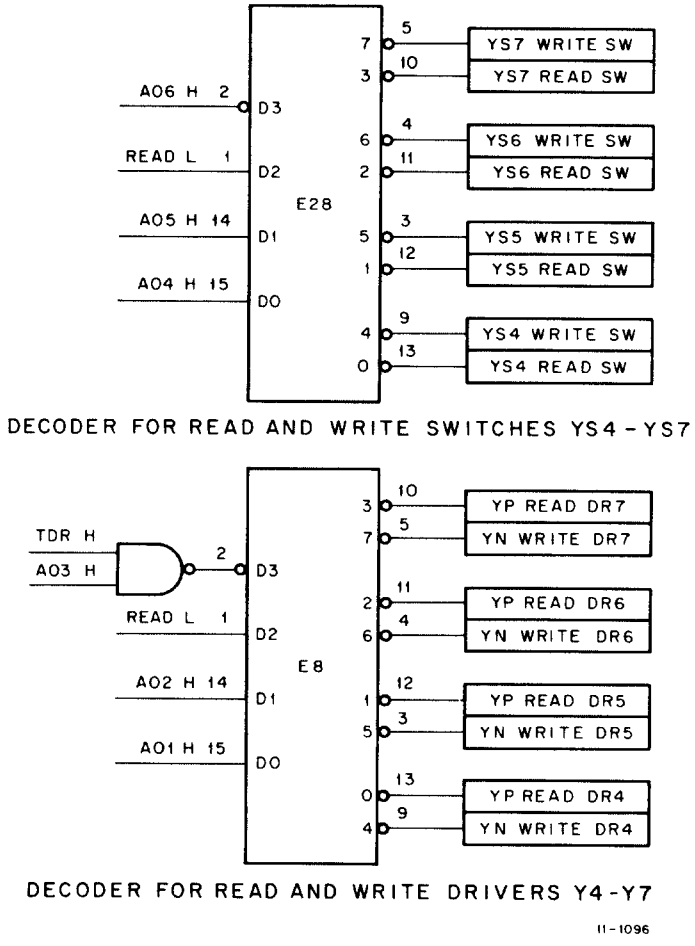


Figure 12-10 Decoding of Read/Write Switches and Drivers Y4-Y7

The four driver decoders (E3, E8, E43, and E46 on drawing G231-0-1, sheets 3 and 4) have a NAND gate connected to input D3. Signal TDR H is an input to each gate; therefore, the driver decoders cannot be enabled unless TDR H is high. This signal is generated on the G231 Driver Module (drawing G231-0-1, sheet 2, coordinates A-8) by ANDing TWID H and READ H or TNAR H and WRITE H.

Each switch/driver is connected to the decoder output through a transformer-coupled base drive circuit. When the decoder output is at ground (low), the switch/driver is turned on; it is turned off when the decoder output is at +3.5V (high). The base drive circuit for write switch YS7 shown in Figure 12-11 is typical.

In this example, the decoder inputs have selected output 7, which is at ground. Current i_1 flows into this decoder output circuit from the +5V supply via resistor R11 and the primary winding (terminals 4 and 3) of transformer T8. The value of i_1 is determined by the value of R11 and the voltage reflected into the transformer primary (approximately 1V). An equal current i_2 is induced in the base-emitter circuit of write switch E29, which is

connected to the transformer secondary winding (terminals 13 and 14). This current turns on E29. All the base current for E29 is provided by this circuit: i_3 is the collector current. When the decoder is turned off, its output pull-up transistor tries to drive the turn-off current i_4 in the opposite direction. This reverse current removes the forward bias from the base of E29 and turns it off. Capacitor C30 allows the decoder to pump reverse current i_4 into the transformer primary; it also speeds up turn-on current i_1. Diode D1 prevents reverse breakdown of the base-emitter junction of E29; it also protects the decoder output.

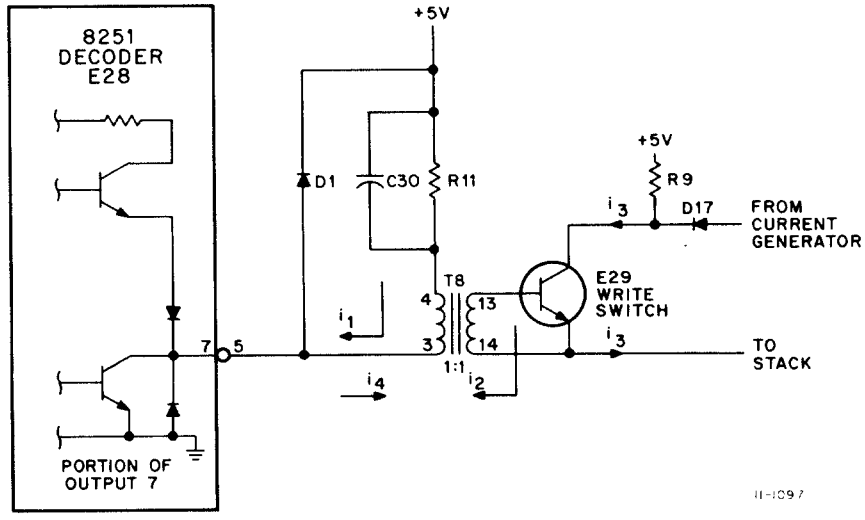


Figure 12-11 Switch or Driver Base Drive Circuit

12.4.3.3 Drivers and Switches – Drivers and switches direct the current through the X- and Y-lines in the proper direction as selected by the read and write operations.

For an 8K memory, 16 pairs of read/write switches and 8 pairs of read/write drivers are provided in the X-axis; 8 pairs of read/write switches and 8 pairs of read/write drivers are provided in the Y-axis. In conjunction with the stack diode matrix (drawing H214-0-1, sheet 2), one driver and any one of 16 switches select 16 lines in the X-axis; one driver and any one of eight switches select eight lines in the Y-axis. This allows selection of 128 lines in the X-axis and 64 lines in the Y-axis. This provides a 128 X 64 matrix that selects any location out of 8192 locations.

For a 4K memory, eight pairs of read/write switches and eight pairs of read/write drivers are provided for each axis (X and Y). One driver and any one of eight switches select eight lines in both axes, which allows selection of 64 lines in each axis and provides a 64 X 64 matrix that selects any location out of 4096 locations. The size of the X-diode matrix for the 4K memory is one half the size of the corresponding matrix for the 8K memory (drawing H213-0-1, sheet 2). In both memories, the diodes prevent sneak currents in the stack and steer all switched current into the selected stack line.

Figure 12-12 is one fourth of a Y-selection matrix showing the interconnection of the diodes and the lines from the switches and drivers. It also shows how four pairs of switches and drivers are connected to select 16 locations. Refer to drawing H213-0-1, sheet 2 for an extension of this method that uses eight pairs of switches and drivers to select 64 locations.

Figure 12-12 shows four pairs of drivers and four pairs of switches for the Y-axis only; polarities are shown for convenience. The diodes are identified to assist in associating them with the drivers and switches. Each line from a twin diode interconnection to a read/write switch pair passes through 64 cores and represents one line on each bit

mat. Assume that a write operation is to be performed and the word address decoders have selected write switch WYS00 and write driver YNWD1. The Y-current generator sends current through write switch WYS00 (conventional flow), which puts a positive voltage on the anodes of diodes 03W, 02W, 01W and 00W. The non-selected write drivers (YNWD3, YNWD2, and YNWD0) provide a positive voltage on the cathodes of their associated diodes (03W, 02W and 00W, respectively), which reverse biases them and prevents conduction. Write driver YNWD1, which has been selected, turns on and makes the cathode of diode 01W negative with respect to the anode that forward biases it. The diode conducts and allows current to flow to write driver YNWD1. A half-select current now flows through this line that links 64 cores per bit mat (1024 total for 16 mats).

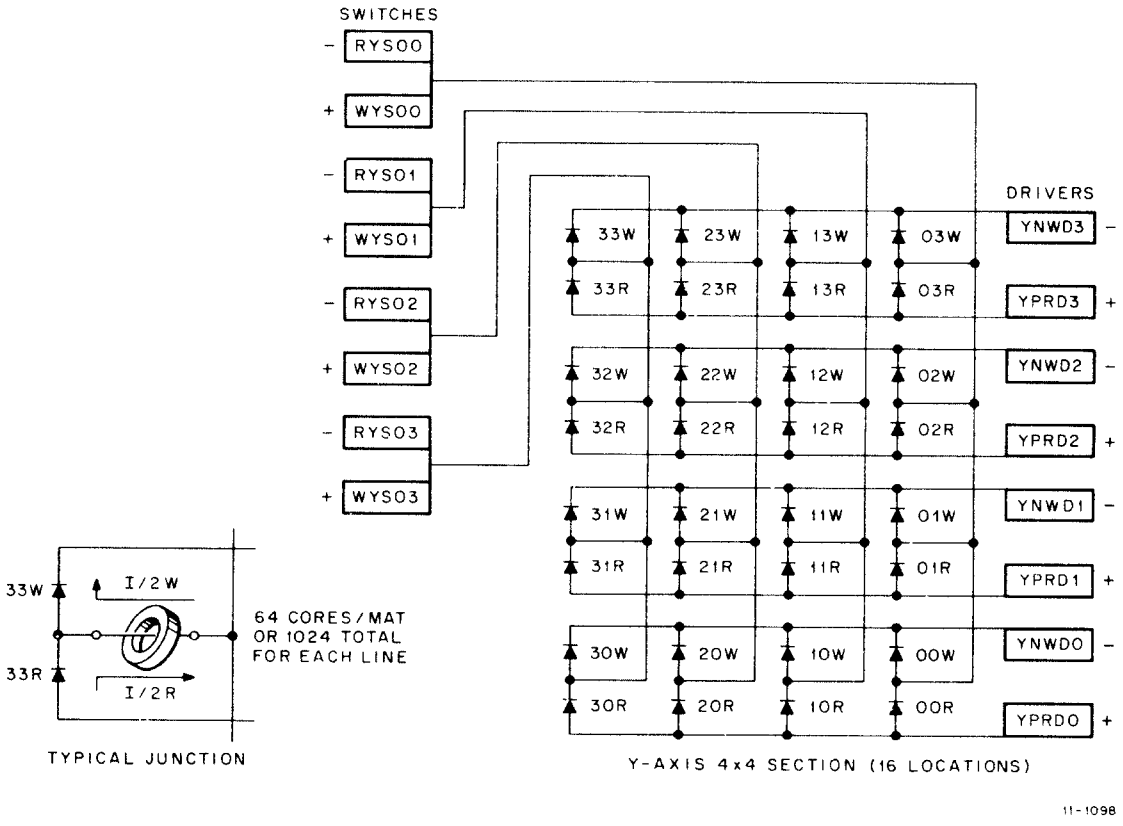


Figure 12-12 Y-Line Selection Stack Diode Matrix

Figure 12-13 is a simplified schematic of two pairs of switches and drivers interconnected with the core stack and current generator. Read/write switches YS07 and read/write drivers YD7 are used as examples. These switches and drivers are chosen for convenience. For a read or write operation, there are 64 switch/driver combinations available on the Y-axis and 128 on the X-axis. For a read operation, decoder E8 selects positive read driver E7 via transformer T3; and decoder E28 selects negative read switch E26 via transformer T7. Both E7 and E26 are turned on when they are selected. E7 conducts and removes the reverse bias on diode D67, which allows current from the Y-current generator to flow through D67, E7, the associated matrix diode, and the cores on the selected line. After passing through the cores, the current flows through E26 and R27 to the -15V line. For a write operation, decoder E28 selects positive write switch E29 via transformer T8; and decoder E8 selects negative write drivers E10 via transformer T4. Both E29 and E10 are turned on. E29 conducts and removes the reverse bias on diode D17, which allows current from the Y-current to flow through D17, E29, and the cores in the opposite direction. After passing through the cores, the current flows through the associated matrix diode, E10, and R140 to the -15V line. Read current flow is shown as a solid line; a broken line shows write current flow.

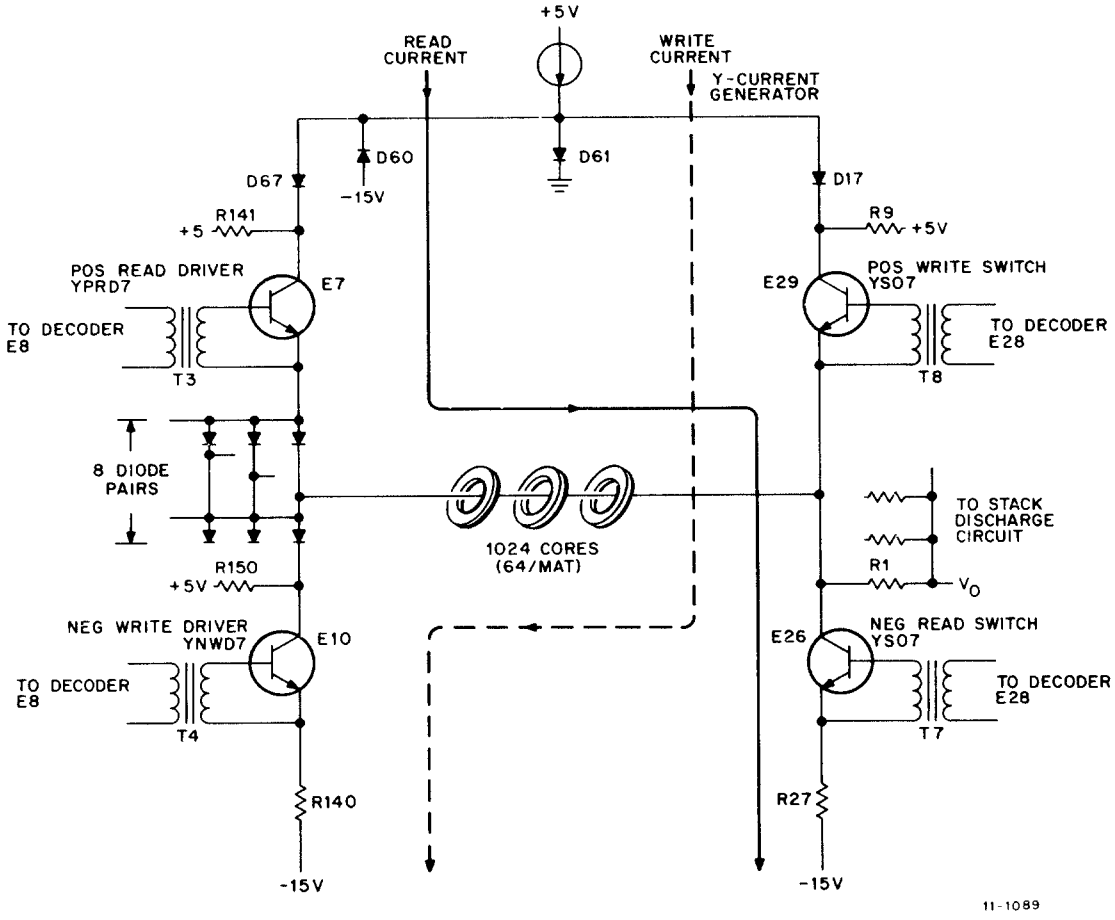


Figure 12-13 Typical Y-Line Read/Write Switches and Drivers

12.4.3.4 Word Address Decoding and Selection Sequence – This paragraph takes a specific word address through the decoding and X- and Y-line selection sequence.

The word address is 017772, and it is assumed that a specific memory bank has been selected. The binary equivalent of the address is shown below. A read operation is to be performed.

ADDRESS BITS A<17:00>

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT POSITION
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	BINARY
0			1			7			7			7			2			OCTAL

11-1173

Bits A (13:01) are used to decode the word address. Bit A01 is sent to the device selector (drawing G110-0-1, sheet 2) and appears at word address flip-flop E11, pin 2 as A01 H (drawing G231-0-1, sheet 2). Bits A (12:02) are sent to the Unibus receivers, which are inputs to the associated word address flip-flops. Bit A13 is not used. The input to the Unibus receiver associated with this bit is connected directly to +5V through jumper J3 (for a 4K memory, J3 is in and J4 is out). Table 12-3 shows the state of bits A (13:01) and the decoding signals generated by the word address flip-flops after they are clocked.

Table 12-3
Word Address Decoding Signals

Address Bit	Unibus Receiver Input	Receiver Output	Flip-Flop State	Flip-Flop Output Signals
A01	L	H	set	A01H = H
A02	H	L	reset	A02H = L
A03	L	H	set	A03H = H, A03L = L
A04	L	H	set	A04H = H
A05	L	H	set	A05H = H
A06	L	H	set	A06H = H, A06L = L
A07	L	H	set	A07H = H
A08	L	H	set	A08H = H
A09	L	H	set	A09H = H, A09L = L
A10	L	H	set	A10H = H
A11	L	H	set	A11H = H
A12	L	H	set	A12H = H, A12L = L
A13	-	-	reset	A13H = L, A13L = H

The output signals from flip-flops A06, A12, and A13 are not used directly from the flip-flops; they are sent to gating logic (E22 and E25) and are ANDed with signal TSS H. In this case, only two out of a possible six signals are generated: A06H is low from E22, pin 12 and (A12H . A13L) L is low from E25, pin 8. These signals and the outputs from the other word address flip-flops are sent to the inputs of the type 8251 decoders to select the appropriate switches and drivers. READ L is an input to each 8251 decoder. A read operation is to be performed; therefore, READ L is low.

The decoders, switches, and drivers are shown in drawing G231-0-1, sheets 3 and 4. Using the decoding signals in Table 12-3 and the operating characteristics of the decoders, it is possible to determine which decoders have been selected for word address 017772. A decoder is selected only when its D3 input is low. In this case, the selected decoders are E34 and E46 for the X-line (drawing G231-0-1, sheet 3), and E23 and E8 for the Y-line (drawing G231-0-1, sheet 4). READ L is low and is sent to input D2 of each decoder; it selects read drivers and switches in this case. To verify this point, refer to the truth table and diagram in Figure 12-9. Decoder inputs D0 and D1 select the particular switch or driver as shown below.

a. Decoder E34
   D1 is high, D0 is high: selects output 3 (pin 10), which is read switch XS07.

b. Decoder E46
   D1 is high, D0 is high: selects output 3 (pin 10), which is read driver XPRD7.

c. Decoder E23
   D1 is high, D0 is high: selects output 3 (pin 10), which is read switch YS03.

d. Decoder E8
   D1 is low, D0 is high: selects output 1 (pin 12), which is read driver XPRD5.

The last step is to follow the outputs of the drivers and switches to the stack diode matrix (drawing H213-0-1, sheet 2). For the X-line, the circuit is from driver XPRD7 to diode junction E7-11, across termination 35 to switch XS07.

For the Y-line, the circuit is from driver YPRD5 to diode junction E4-9, across termination 15 to switch YS03. The termination indicates the point on the stack printed circuit board where the X- or Y-line is soldered. Physically, the wire that is connected across the termination is strung through 64 cores per bit mat (total of 1024 cores in series for 16-bit memory).

12.5 READ/WRITE CURRENT GENERATION AND SENSING

In addition to the addressing and control logic, four functional units are involved in generating current to switch the cores and detect their state. The X- and Y-line current generators supply the drive current (via switches and drivers); the inhibit drivers allow 0s to be written during a write operation; the sense amplifiers detect 1s during a read operation; and the memory data register (MDR) temporarily stores data to be written or data that has been read from the memory. The following paragraphs describe each functional unit and their interrelationship.

12.5.1 Read/Write Operations

The read/write operations are discussed in terms of the interrelation of the current generator, inhibit drivers, sense amplifiers, and memory data register. Details of operation of each functional unit are discussed in subsequent paragraphs. Several control signals are mentioned; however, details of their generation and timing are described in Paragraph 12.8.

For clarity, one data bit (D07) of the selected word is discussed and the text is referenced to Figure 12-14, which is a simplified block diagram. Detailed logic for the memory data register (MDR), Unibus receivers and drivers, sense amplifiers, and inhibit drivers for all 16 data bits is shown on drawing G110-0-1, sheets 3 and 4.

During a read operation, half-select currents flow in the X- and Y-lines for the selected word in each bit mat. These currents flow opposite to the write currents; therefore, cores in the 1 state are switched to the 0 state, and cores in the 0 state are unchanged. Switching the core from the 1 state to the 0 state induces a voltage pulse in the sense winding. This pulse is detected by sense amplifier E52 as a differential voltage on input pins 6 and 7 that exceeds the threshold reference voltage. This pulse is amplified and when STROBE O H is generated at pin 11, the output of sense amplifier E52 goes high. Just prior to the strobe signal, the control logic generates RESET O L, which clears (resets) flip-flop E54. The sense amplifier output is inverted by E56 and sent to the preset input (pin 10) of MDR flip-flop E54. A low on the preset input sets the flip-flop: its 1-output (pin 9) is a high and its 0-output (pin 8) is a low. The high from pin 9 of the flip-flop is sent to input pin 1 of the Unibus driver E21. The other input to this gate is the data out signal. When the control logic generates DATA OUT H, the output of E21 is low (logical 0 for memory logic and logical 1 for Unibus logic). This is the readout of bit D07 and is sent to the requesting device via the Unibus. Timing diagrams for the sense operation are also shown in Figure 12-14.

The read operation is destructive: all cores at the specified location are now 0. The data that was read must be restored by a write operation, which immediately follows the read operation. Flip-flop E54 is still in the set state; therefore, its 0-output (pin 8), which is low, is sent to input pin 9 of NAND gate E53. The control logic generates the inhibit driver control signal TINHO H, which is the other input to gate E53. The gate is not asserted (pin 8 is high), and the inhibit driver is not turned on. With no inhibit current in the inhibit line to oppose the half-select Y-line current, a 1 is written back into the appropriate cores.

In this example, if bit D07 is a 0 in core, it does not switch during the read operation and the output of sense amplifier E52 does not go high. Flip-flop E54 remains cleared (reset): its 1-output (pin 9) is low and its 0-output (pin 8) is high. When the control logic generates DATA OUT H, the output of Unibus driver E21 is high (logical 1 for memory logic and logical 0 for Unibus logic). The 0-output of flip-flop E54, which is high, is sent to NAND gate E53. During the subsequent write operation, TINHO H is generated, producing a low output signal at E53, pin 8 to activate the inhibit driver which in turn produces a current that opposes the Y-line current and prevents a 1 from being written into this bit of the selected word.

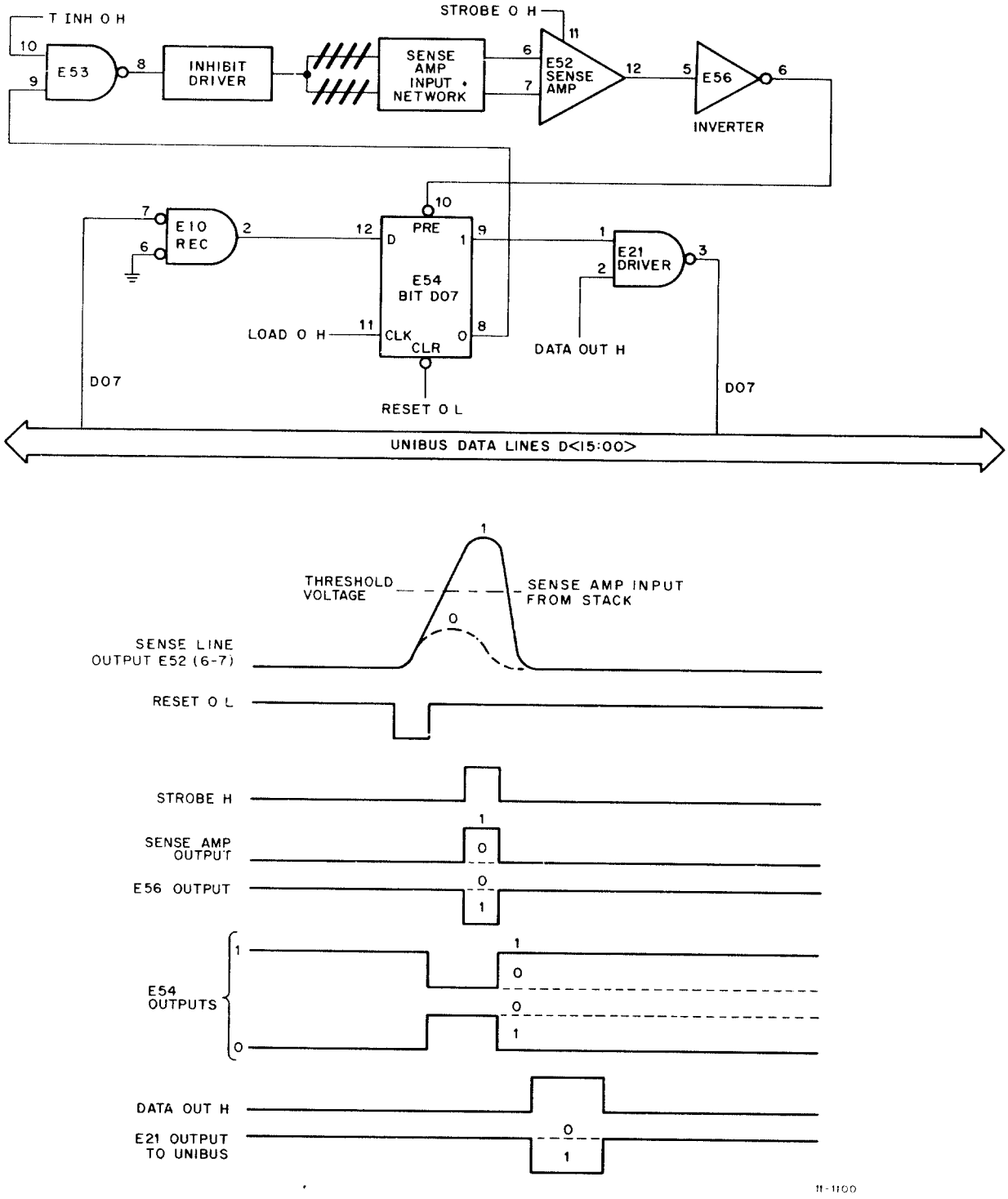


Figure 12-14 Interconnection of Unibus, Data Register, Sense Amplifier, and Inhibit Driver

The read/write operation that has been discussed is a read/restore operation (DATI). The requesting device wants to read a word from memory, and as an internal requirement, the memory must restore the word by writing it back into core. In this case, the MDR flip-flops are preset by the sense amplifier outputs when 1s are read from the core. The MDR flip-flop outputs are used in the subsequent write (restore) operation to control the inhibit drivers. If the requesting device wants to write a word into memory (DATO), it must load the data into the MDR flip-flops. The

requesting device then asserts the data on the Unibus, from which it is picked off via Unibus receivers. In this example, bit D07 is sent to pin 7 of Unibus receiver E10. Bit D07 is inverted by the receiver and sent to the D-input (pin 12) of flip-flop E54. At the start of the DATO operation, the control logic generates LOAD O H, which clocks the flip-flop. If the D-input is high, E54 is set and its 0-output is low. Control gate E53 is not asserted by TINHO H, and the inhibit driver is not turned on. A 1 is written into the selected core. If the D-input is low, E54 is reset and its 0-output is high. Control gate E53 is asserted by TINHO H, and the inhibit driver is turned on. A 0 is written into the selected core. Because RESET and STROBE are inactive in this mode, the read operation is used only to magnetically clear all the cores to the 0 state.

12.5.2 X- and Y-Current Generators

Two identical current generators are provided: one each for the X- and Y-drive lines. They generate the current pulses that are used during read and write operations to switch the cores. The current generators and associated reference voltage supply are shown in drawing G231-0-1, sheet 2. Figure 12-15 shows the Y-current generator and reference voltage supply.

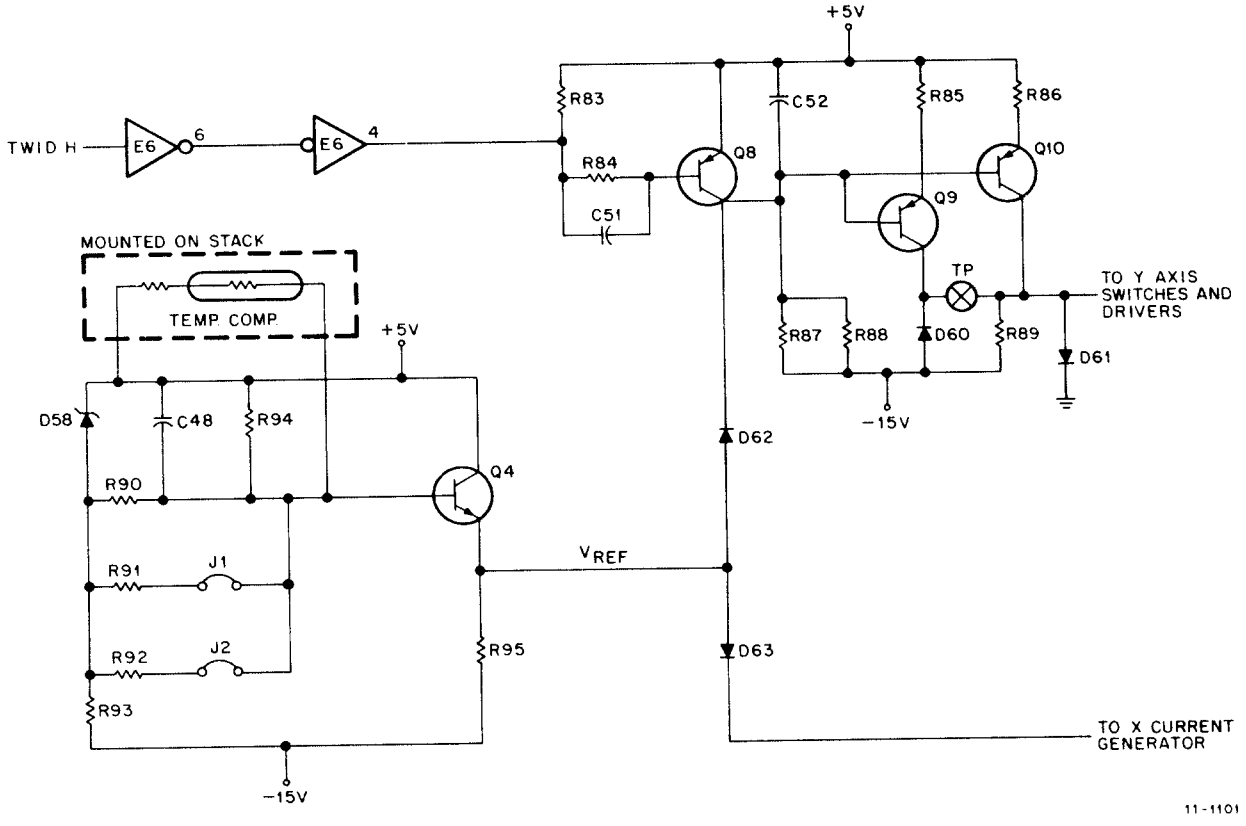


Figure 12-15 Y-Current Generator and Reference Voltage Supply

Optimum core switching requires repeatable current pulses of constant amplitude with a linear rise time. The current generator and reference voltage circuit provide current pulses that meet these requirements. The amplitude of the output current pulse is determined by the reference voltage circuit; the rise time is determined by an RC circuit in the current generator; and pulse duration is determined by the length of the triggering pulse TWID H.

During the quiescent state of the current generator, input transistor Q8 is on; its collector voltage is 4.7V, and it is connected to the cathode of diode D62, which reverse biases it. The anode of D62 is connected to the emitter of transistor Q4, which is the output of the reference voltage circuit. In this state, D62 blocks the output from the reference voltage circuit to the current generator. With Q8 on, both output transistors Q9 and Q10 are turned off, and the current generator is off.

Operation of the current generator is triggered by a high TWID H signal from the control logic. TWID H is double inverted by two E6 inverters and sent to the base of Q8, which turns it off. When Q8 is cut off, capacitor C52 starts charging, which provides base drive to output transistors Q9 and Q10 and they begin to conduct. With Q8 off, its collector goes negative until it reaches the forward bias level of D62, which is the value of the reference voltage minus the voltage drop across D62. The rise time of the current pulse is determined by the time constant of C52, R87, and R88. The amplitude of the pulse is determined by the value of the reference voltage. When TWID H goes low again, the current generator is turned off and the output pulse is terminated.

A resistor network in the base circuit of Q4 (in the reference supply) is used to set the amplitude of the current generator to approximately 410 mA. The total resistance of parallel network R90, R91, and R92 is changed by the configuration of jumpers J1 and J2. The amplitude of the current generator output pulse is factory set as close as possible to 410 mA at 25°C. It should not be changed in the field.

The base circuit of Q4 is temperature compensated by a resistor and thermistor that are mounted on the stack. This ensures that the amplitude of the current generator output pulse remains within specified tolerances over a temperature range of 0°C to 50°C. This temperature compensation is approximately -0.8 mA/°C.

12.5.3 Inhibit Driver

A detailed schematic of the inhibit driver for bit D07 is shown in Figure 12-16; it is typical of all 16 inhibit drivers (drawing G110-0-1, sheets 3 and 4).

When the inhibit driver is off, none of the currents shown in the schematic are flowing. Transistor Q7 is held off by the negative voltage on its base. The output of NAND gate E53 goes low (ground) when this inhibit driver is selected. Current i_1 flows into the output circuit of E53 from the +5V supply via resistor R87 and the primary winding (terminals 15 and 16) of transformer T8. An equal current is induced in the base-emitter circuit of Q7, which is connected to the transformer secondary winding (terminals 1 and 2). This base current overcomes the reverse bias voltage and turns on Q7. Current i_1 and therefore induced-current i_2 are determined by resistor R87 and the reflected base-emitter voltage V_{be} of Q7. When Q7 is turned on, current flows from ground through Balun transformer T7, isolation diodes D13 and D14, and the sense/inhibit winding to the common inhibit terminal (07IN). The Balun transformer balances the two inhibit half-currents. At terminal 07IN, the full inhibit current flows through resistor R72 and Q7 to -15V. The value for the inhibit current is calculated as follows:

$$i_{inh} \frac{\cong 15V - V_{ce\ sat\ Q7} - V_{be\ diodes}}{R72 + R_{core\ mat}}$$

$$\underline{\cong 15 - 0.8 - 1.2} = \frac{13}{17.5} = 740\ mA$$

Each leg of the sense/inhibit winding sees half the inhibit current: approximately 370 mA. Capacitor C55 decreases the rise time of the current.

The inhibit driver is turned off when the output (pin 8) of gate E53 goes from low to high. At turn-off time, the back emf caused by the stack inductive reactance tries to drive the collector of Q7 highly positive; however, diode D43 clamps this voltage to ground. When the output of E53 goes high (approximately +3.2V), its output pull-up transistor (an integral part of the gate circuit) tries to drive the turn-off current i_4 in the opposite direction through the transformer primary winding. An equal current induced in the secondary winding removes the forward bias from

the base of Q7 and turns it off. With Q7 off, all dynamic current flow ceases in the circuit and the negative voltage on the base of Q7 keeps the circuit turned off until the output of gate E53 goes low again.

Capacitor C74 allows the gate to pump reverse current i_4 into the transformer primary; it also helps to decrease the turn-on time of Q7. Diode D59 prevents reverse breakdown of the emitter junction of Q7.

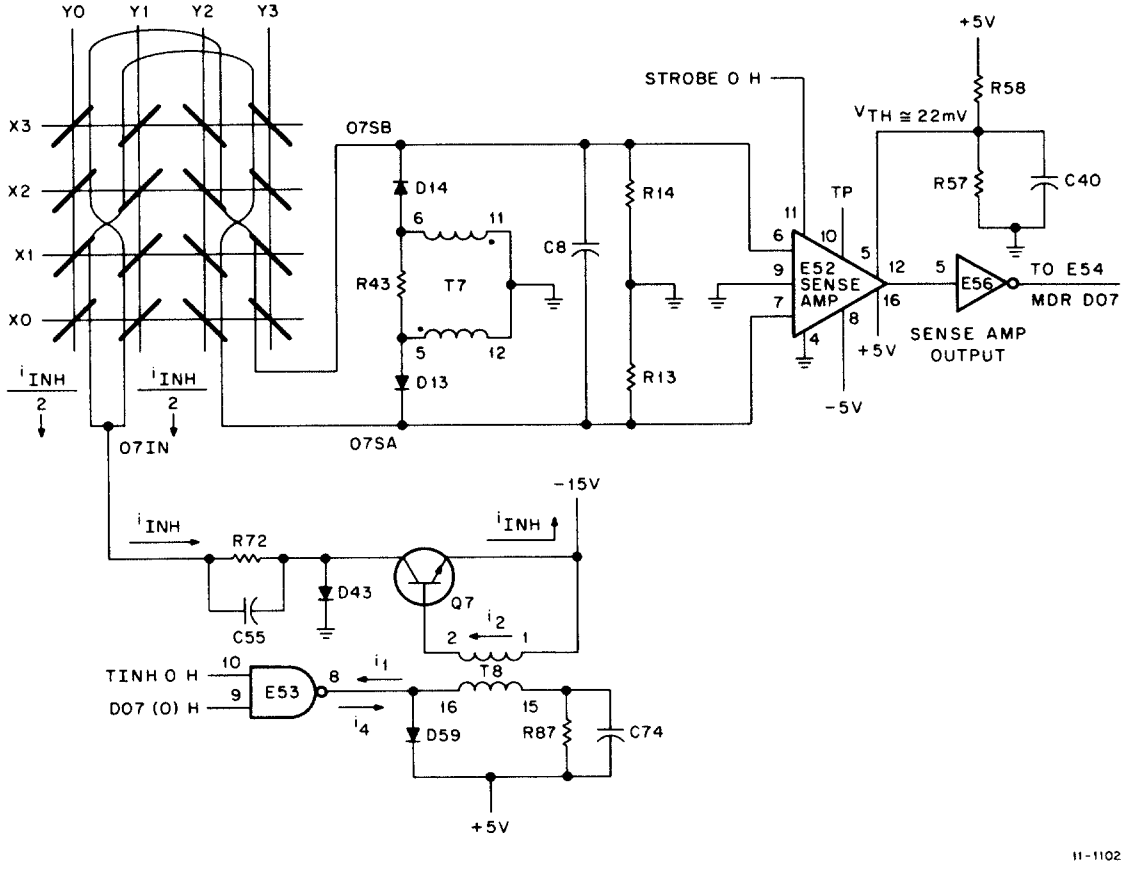


Figure 12-16 Sense Amplifier and Inhibit Driver

12.5.4 Sense Amplifier

A detailed schematic of the sense amplifier circuit for bit D07 is shown in Figure 12-16; this circuit is typical of all 16 sense amplifier circuits (drawing G110-0-1, sheets 3 and 4). The circuit consists of the sense amplifier, terminating network for the sense/inhibit winding, and threshold voltage network.

The sense amplifier input (E52, pin 6 and 7) is across the sense/inhibit winding (points 07SB and 07SA). Resistors R13 and R14 are matched to terminate the sense/inhibit line in the desired impedance. Practically speaking, during the sense operation, the inhibit driver connection is an open circuit through the driver transistor Q7. The effect of the inhibit driver circuit, Balun transformer T7, and isolation diodes D13 and D14 can be ignored during the sense operation, because the diodes are reverse biased.

Sense amplifier E52 is one half of a dual IC package (type 7528). A simplified block diagram of the package is shown in Figure 12-17. The two identical circuits are marked 1 and 2. Each one consists of a preamplifier and sense

amplifier. The output of the preamplifier is available as a test point to observe the amplified core signal and to facilitate accurate strobe timing. Both circuits share a reference voltage (or threshold voltage) amplifier (pins 4 and 5). In this application, pin 4 is grounded and a positive threshold voltage of approximately 20 mV is supplied to pin 5. This voltage is obtained from the +5V supply through resistor voltage divider R57 and R58; C40 is a bypass capacitor. Operation of the sense amplifier is discussed in Paragraph 12.5.1.

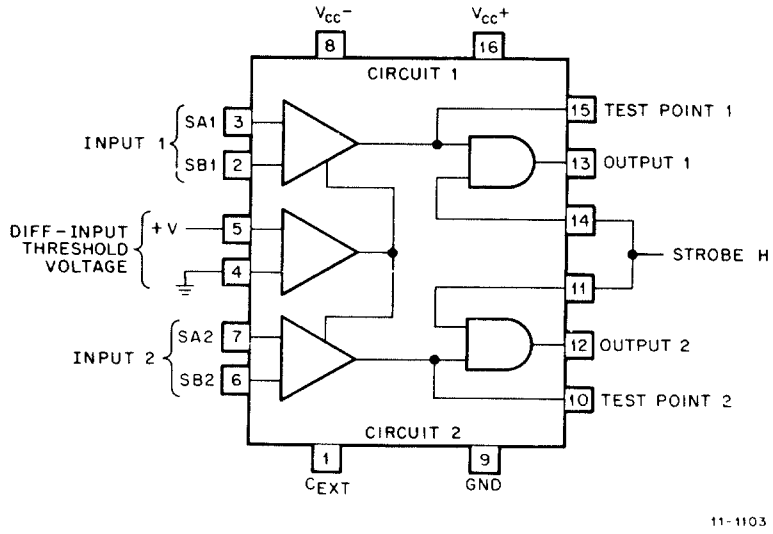


Figure 12-17 Type 7528 Dual Sense Amplifiers With Preamplifier Test Points

12.5.5 Memory Data Register

The memory data register (MDR) is a 16-bit flip-flop register that is used to store a word after it is read out of the memory; or to store a word from the Unibus prior to its being written into the memory. The MDR is composed of eight 74H74 dual high-speed D-type flip-flops: bits D00-D07 are shown in drawing G110-0-1, sheet 3 and are identified as E54, E57, E60, and E63; bits D08-D15 are shown in drawing G110-0-1, sheet 4 and are identified as E42, E45, E48, and E51.

At the start of a memory operation, the MDR is cleared directly via the clear input (pin 1 or pin 13) of each flip-flop: the clear signal is RESET 0 L for bits D00-D07 and RESET 1 L for bits D08-D15.

The operation of the MDR during a read/restore operation (DATI) and a write operation (DATO) is discussed in Paragraph 12.5.1.

12.6 STACK DISCHARGE CIRCUIT

The stack discharge circuit assists the stack capacitance in recovering and shortens the rise time of the stack current. It also reduces unwanted currents in the seven unselected lines associated with the selected driver.

Figure 12-18 shows the stack discharge circuit. Its output is taken from the emitter of transistor Q2 and goes to the junction of each X- and Y-read/write switch pair via a resistor. This common interconnection is labeled V_0. It is desired that $V_0 \cong 0V$ (ground) during a read operation; and $V0 \cong -15V$ during a write operation. The effective stack capacitance associated with each line is shown as C_{stack}.

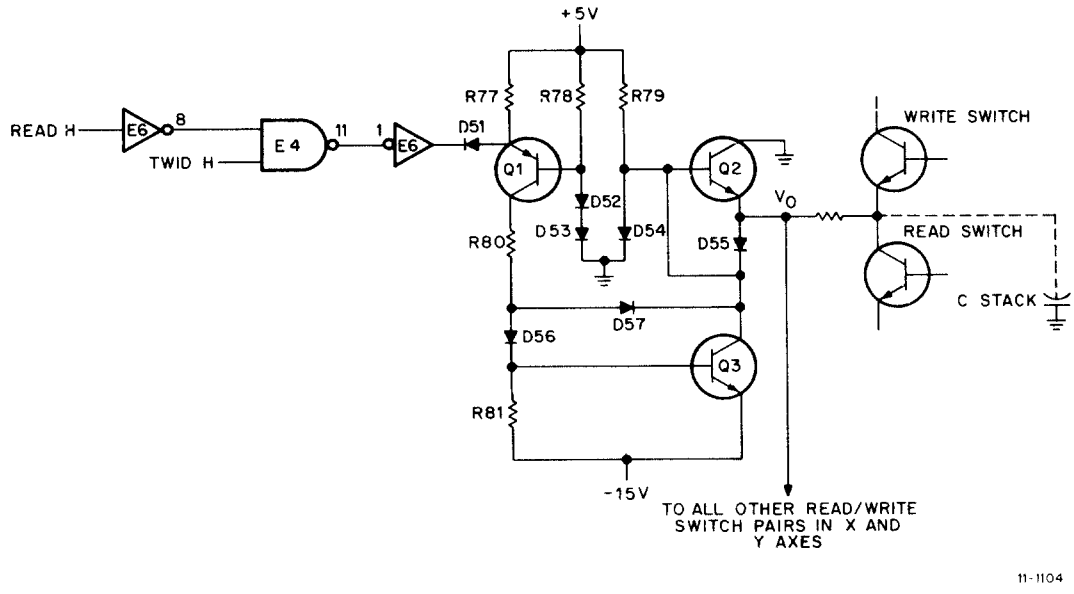


Figure 12-18 Stack Discharge Circuit

During a write operation, READ H is low; it is inverted and ANDed with TWID H at NAND gate E4. The low output (pin 11) of E4 is inverted by E6 and sent to the cathode of diode D51, which reverse biases it. The emitter of Q1 becomes more positive, overcomes the constant positive base bias, and turns on transistor Q1. When Q1 conducts, it provides base drive for Q3, which also turns on. When Q3 conducts, it reduces the base drive on Q2 and it turns off. The emitter voltage of Q2 goes to approximately -14V, which is V_0 on the switch node for the stack. Diode D57 prevents hard saturation of Q3; diode D55 holds Q2 off. During a write operation, V_0 = -14V and the stack discharge circuit is considered to be turned on (input transistor Q1 is on).

During a read operation, READ H is high: it is inverted and ANDed with TWID H at NAND gate E4. The gate is not asserted and its output (pin 11) is high. This signal is inverted by E6 and sent to the cathode of diode D51, which forward biases it. The voltage on the emitter of Q1 produced by the current through R77 and D51 is not enough to overcome the constant positive bias and Q1 is turned off. With Q1 off, Q3 looses its base drive and turns off. Now, D55 cannot hold Q2 off. As long as the stack capacitance is charged negatively, base current exists for Q2 and it remains on. The stack capacitance now charges in the positive direction until it reaches ground potential. During a read operation, $V_0 \cong 0V$ and the stack discharge circuit is considered to be off (input transistor Q1 is off).

Figure 12-13 shows how the stack discharge circuit reduces unwanted currents on the seven unselected lines associated with the selected driver.

During a read operation, the stack discharge circuit is off and V_0 = 0V. The current generator drives the read driver node of the stack towards ground; the current generator output is clamped to ground by diode D61. The anodes of the eight read diodes are at ground. The stack discharge circuit is on and the cathodes of the seven unselected diodes are also at ground, which back biases them off. The read switch pulls the cathode of the selected line towards -14V, which forward biases it and allows conduction through the diode. Current flows only through the selected line. Reverse biasing of the diodes in the unselected lines prevents current from flowing between the unselected nodes and the selected read driver. The stack discharge circuit performs the same task during the write operation by back biasing the anodes of the diodes in the unselected lines with -14V.

12.7 DC LO CIRCUIT

A circuit on the G231 Driver Module (drawing G231-0-1, sheet 2) opens the -15V supply line to the current generators when power is interrupted to the power supply. When power is interrupted, the +5V supply is lost and the operation of all logic is indeterminate. In this state, it is necessary to cut off the -15V supply to the X- and Y-line current generators to prevent them from destroying stored data. The circuit that performs the -15V cutoff is called the DC LO circuit (Figure 12-19).

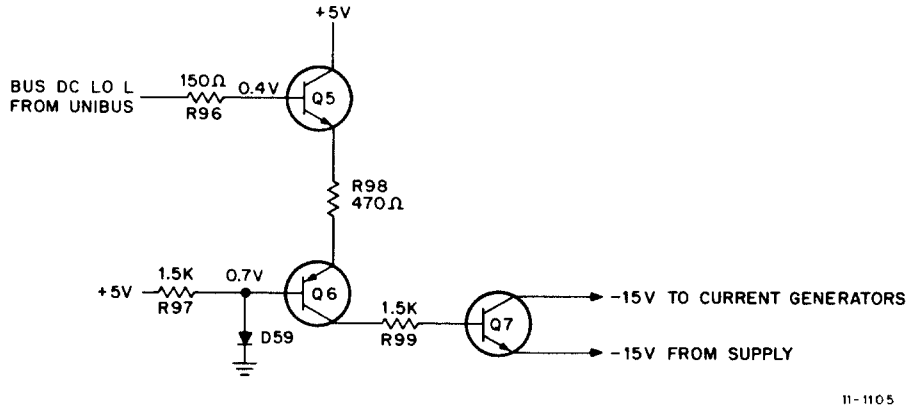


Figure 12-19 DC LO Circuit, Schematic Diagram

The -15V supply for the X- and Y-line current generators passes through transistor Q7 in the DC LO circuit. Q7 must be turned on for the -15V to reach the current generators. The circuit monitors BUS DC LO L from the power supply via the Unibus. This signal is sent to the base of transistor Q5. When power is on, BUS DC LO L is high (not asserted).

The voltage across R96 forward biases Q5 and it turns on, which turns on Q6. The conduction through Q5 and Q6 forward biases Q7 which turns it on. The -15V flows through Q7 to the X- and Y-line current generators.

When power is interrupted, BUS DC LO L goes low (asserted). Q5 is now reverse biased and it turns off, which turns off Q6. With Q5 and Q6 off, Q7 is also turned off, which opens the -15V line to the current generators. This circuit still functions when BUS DC LO L is asserted even if the +5V supply drops to zero.

12.8 OPERATING MODE SELECTION LOGIC

When the memory is addressed by the master device, one of four bus transactions is selected. The transaction (or operation) selected is determined by the states of control bits C01 and C00 and address bit A00 as placed on the Unibus by the master device. Table 12-4 shows the states of these bits for each transaction.

The logic that decodes the mode and byte control bits is shown in drawing G110-0-1, sheet 2; it appears at the bottom of the sheet and is identified as the byte masking logic. Bits BUS C01, BUS C00, and BUS A00 are taken from the Unibus to three E29 receivers. One input of each gate associated with C01 and C00 is connected to the output of the PROTECT LOW gate (E29 pin 3). Both inputs to this gate are tied to +5V so that its output is always low. For troubleshooting purposes, a jumper (W11) can be installed that makes the gate output high, which allows only DATI operations to be performed regardless of the states of bits C01 and C00. This jumper hardwires the memory as a read-only device.

Table 12-4
Selection of Bus Transactions

Transaction	Mnemonic	Mode Control		Byte Control A00	Function
		C (01:00)	Octal		
Data In	DATI	00	0	X	Data from memory to master. Memory performs operations.
Data In, Pause	DATIP	01	1	X	Data from memory to master. Restore operation is inhibited. Must be followed by DATO or DATOB: Read operation is inhibited.
Data Out	DATO	10	2	X	Data from master to memory (words).
Data Out, High Byte	DATOB	11	3	1	Data from master to memory. High byte on data lines D (15:08).
Data Out, Low Byte	DATOB	11	3	0	Data from master to memory. Low byte on data lines D (07:00).

The outputs of the three E29 receivers (C01, C00, and A00) are sent to the byte masking logic to generate LOAD 0 H and LOAD 1 H and to qualify a group of gates, which are enabled by control signals to generate RESET 0 L, RESET 1 L, STROBE 0 H, STROBE 1 H, and DATA OUT H. The logic also conditions the D-input of the PAUSE flip-flop (E4, pin 12) to allow it to be set or reset. It also applies conditioning signals to the wired-AND that provides the clocking signal to the slave synchronization (SSYN) flip-flop. The PAUSE flip-flop and the SSYN flip-flop are part of the control logic.

The signals generated for each bus transaction are shown in Table 12-5. The memory operational sequences are discussed in subsequent paragraphs. To avoid confusion in interpreting the transactions listed in Table 12-5, the purpose of the PAUSE flip-flop is discussed briefly. During DATIP, the PAUSE flip-flop is set during the read operation, which inhibits the restore (write) operation. The DATIP must be followed by a DATO or DATOB on the same address. The DATO or DATOB that follows a DATIP is shorter than a standard DATO or DATOB because the initial read operation is eliminated. In Table 12-5, the suffix PAUSE L identifies the standard transactions; the suffix PAUSE H identifies the DATO and DATOB transactions that must follow a DATIP.

12.9 CONTROL LOGIC

The control logic generates the precisely timed signals that initiate and stop the memory operations that are requested as a result of the decoding of the bus transaction. The heart of the control logic is the delay line timing circuit. For better understanding, the timing circuit, slave sync circuit, pause/write restart circuit, and strobe generating circuit are described separately. Each bus transaction is also discussed in detail. The discussion is to the detailed logic level but the signals are not traced through each component. The text is referenced to logic drawing G110-0-1, sheet 2 and the timing diagrams in drawing MM11-L-3.

Table 12-5
Generation of Memory Operating Signals

Mode	Byte Control A00	Mode Control C01	Mode Control C00	State of PAUSE Flip-Flop	Signals Generated							Operation Sequence
					STROBE 0	STROBE 1	RESET 0	RESET 1	LOAD 0	LOAD 1	DATA OUT H	
DATI	X	0	0	Reset	X	X	X	X			X	Read-Restore.
DATIP	X	0	1	Reset-Set	X	X	X	X			X	Read-Pause. Restore inhibited by PAUSE flip-flop.
DATO PAUSE L	X	1	0	Reset					X	X		Clear-Write.
DATO	X	1	0	Set					X	X		Write. Must follow DATIP.
DATOB PAUSE L	0	1	1	Reset		X		X	X			Clear-Write selected byte 0. Clear-Restore non-selected byte 1.
DATOB PAUSE H	0	1	1	Set		X		X	X			Write selected byte 0. Restore non-selected byte 1. Must follow DATIP.
DATOB PAUSE L	1	1	1	Reset	X		X			X		Clear-Write selected byte 1. Clear-restore non-selected byte 0.
DATOB PAUSE H	1	1	1	Set	X		X			X		Write selected byte 1. Restore non-selected byte 0. Must follow DATIP.

12.9.1 Timing Circuit

The heart of the memory control logic is the timing circuit. When activated, it generates a series of precisely timed signals that control memory operation. The major component of the timing circuit is a delay line (DL1) with multiple 25-ns taps (drawing C110-0-1, sheet 2). The delay line outputs are gated to produce the control signals. Figure 12-20 shows the timing of the delay line outputs and the timing of the control signals obtained by gating these outputs. A brief statement of the function of each control signal is included. Absolute timing is obtained from the engineering timing diagram (drawing MM11-L-3). The discussion is referenced to Figure 12-20 and the control logic drawing G110-0-1.

When the system is turned on, the processor asserts BUS INIT L on the Unibus. This initializing signal is sent to pins 6 and 7 of bus receiver E7. It is inverted by E7 to produce a high, which is sent to pins 9 and 10 of the memory select reset (MSEL RESET) gate E16. The output (pin 8) of E16 is low and is used to clear (reset) MSEL flip-flop E2 via the 100-ns delay DL3. The output of E7 is also inverted by E18 to provide a low that clears read/write (R/W) flip-flop E3. The output of E7 is also inverted by E15 to provide a low that clears PAUSE flip-flop E4. The low

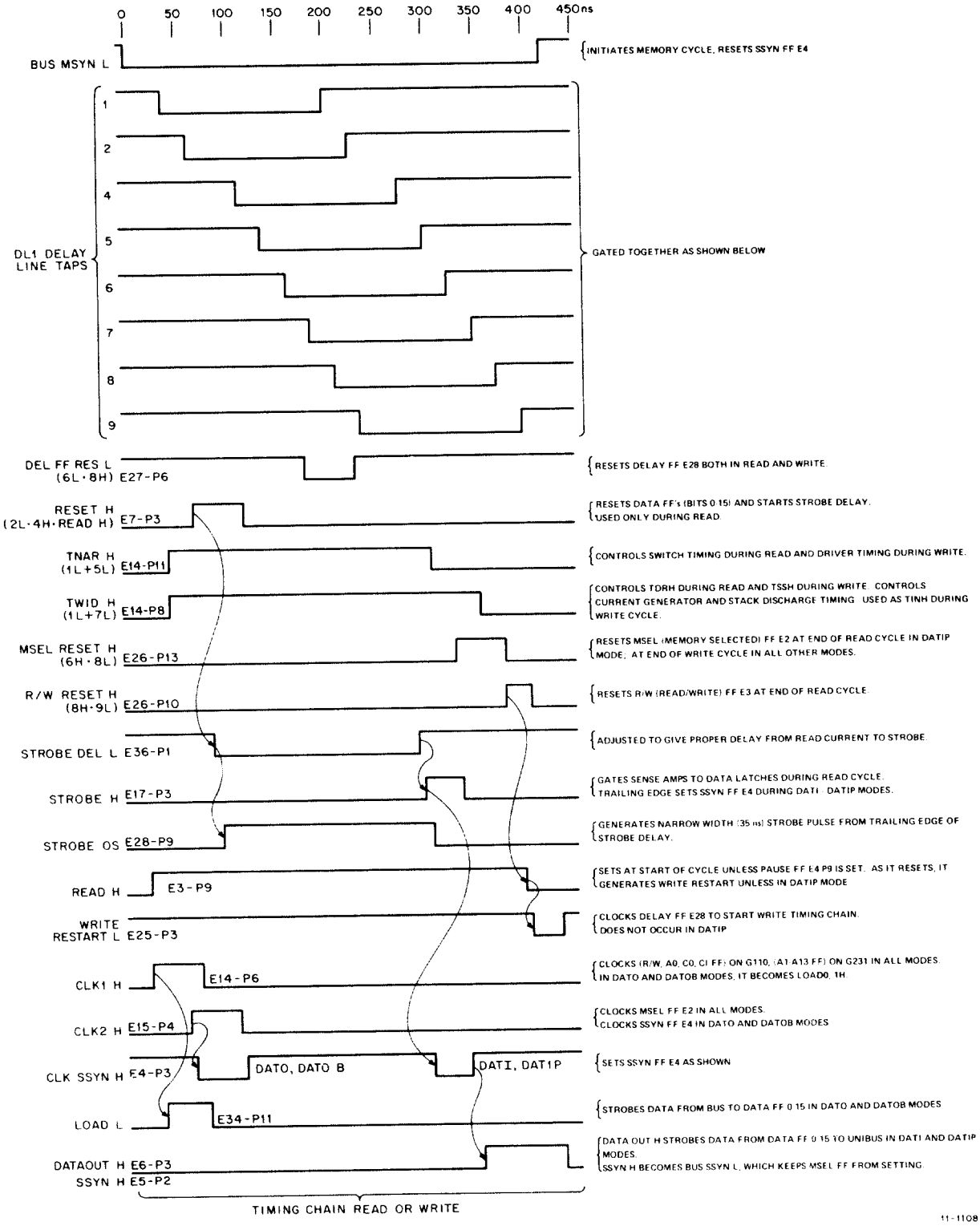


Figure 12-20 Basic Timing and Control Signal Functions

output of E15 is double inverted by two E38 gates to clear the DEL flip-flop E28. The master places the address, mode control state, and data (if required) on the Unibus. The device address is decoded and DSEL H is generated and sent to pin 13 of E1, which is one of four input signals (pins 10, 11, 12, and 13). Pin 11 is high via the 0-output of MSEL flip-flop E2. SSYN flip-flop E4 is preset, making pin 10 of E1 high via its 1-output (pin 5). When the master asserts BUS MSYN L to bus receiver E23, pin 12 of E1 is high also. The output of E1 (pin 8) goes low and is sent to pin 13 of E5, pins 4 and 5 of E14, and pin 1 of delay line DL2. E14 inverts the low from E1 to start the positive CLK 1 H pulse. DL2 provides a 30-ns delay for the low signal from E1, which is inverted by E15 to start the positive CLK 2 H pulse. The output (pin 3) of DL2 is also sent to the preset input (pin 4) of MSEL flip-flop E2, and pin 6 goes low which in turn is fed back to pin 10 of E1 to disable it. The output (pin 8) of E1 is now high, and this signal terminates both clock pulses (CLK 1 H and CLK 2 H) via gates E14 and E15. These pulses are approximately 50-ns wide.

Gate E5 also inverts the low from E1 because pin 12 (WRITE RESTART L) of E5 is high. The positive transition at the output (pin 11) of E5 clocks delay (DEL) flip-flop E28 which sets it. Pin 5 of E28 is high and is connected to pins 1 and 2 of DL1 driver gate E34. The low from the E34 output (pin 3) is the input to delay line DL1. This signal remains low for approximately 225 ns until DEL flip-flop E28 is cleared by DELAY FF RESET L. This provides a negative pulse that propagates through the delay line and can be picked off at 25-ns intervals.

DL1 taps 2, 4, 5, 6, 7, 8, and 9 are used to generate control signals. Figure 12-20 depicts each control signal and relates it to logic drawing G110-0-1, sheet 2.

DELAY FF RESET

Tap 6L is inverted by E15 and sent to pins 3 and 5 of 3-input NAND gate E27; the third input (pin 4) is tap 8H. The output (pin 6) of E27 clears the DEL flip-flop E28; however, it is ORed with INIT L in gate E28 (pins 9 and 10) and inverted by E38, pin 11 so that either (6L . 8H) or BUS INIT L can produce DELAY FF RESET L, which clears E28 via its clear input (pin 1). This signal is generated in both read and write operations.

RESET H

Tap 2L, tap 4H, and signal READ H are gated to generate RESET H, which triggers the strobe delay circuit and generates RESET 0 L and RESET 1 L during the read operation only. Tap 4H and READ H (high during read operation) are ANDed at pins 10 and 9 of E17. The low output of E17 is ANDed with tap 2L in gate E7. The high output (pin 3) is RESET H.

TWID H and TNAR H

The 0-output of DEL flip-flop E28 is ORed with tap 5L and tap 7L in separate gates (E14) to produce signals TWID H and TNAR H. Tap 5L is sent to pin 13 of E14; the other input to this gate (pin 12) is from the 0-output of DEL flip-flop E28. Tap 7L is sent to pin 10 of another E14 gate; pin 9 of this gate is also connected to the 0-output of DEL flip-flop E28. These gates are 2-input NAND gates (type 7437); however, they are shown as logically equivalent negative-input OR gates, because it is desired to have them asserted high (logical 1) when TWID H or TNAR H is asserted.

At the start of a read or write cycle, just before E28 is set, TNAR and TWID are low because both inputs to each gate are high. E28 is set and pins 12 and 9 of E14 go low; TNAR and TWID are both high, which starts the positive TNAR and TWID pulses simultaneously. When taps 5 and 7 go low (E28 is still set), TNAR and TWID remain high. At the end of the read or write cycle, E28 is cleared (taps 5 and 7 are still low) and TNAR and TWID still remain high. When tap 5 is high again, TNAR goes low because both inputs (pins 12 and 13) of E14 are high. This terminates the positive TNAR pulse. Approximately 50-ns later, tap 7 is high again and TWID goes low, terminating the positive TWID pulse. In summary, TNAR H and TWID H are started together by setting DEL flip-flop E28 before taps 5 and 7 are low; TNAR H and TWID H are not effected when taps 5 and 7 go low. Signals TNAR H and TWID H are terminated when taps 5 and 7 return high. The intervening clearing of E28 does not affect TNAR H or TWID H.

Signals TNAR H and TWID H provide various control functions related to the operation of the switches, drivers, current generators, inhibit drivers, and stack discharge circuit. At this point, the discussion digresses to follow TNAR H and TWID H through some additional logic in order to understand their functions. The logic is spread throughout several engineering drawings. To simplify the discussion, all the logic is shown in Figure 12-21.

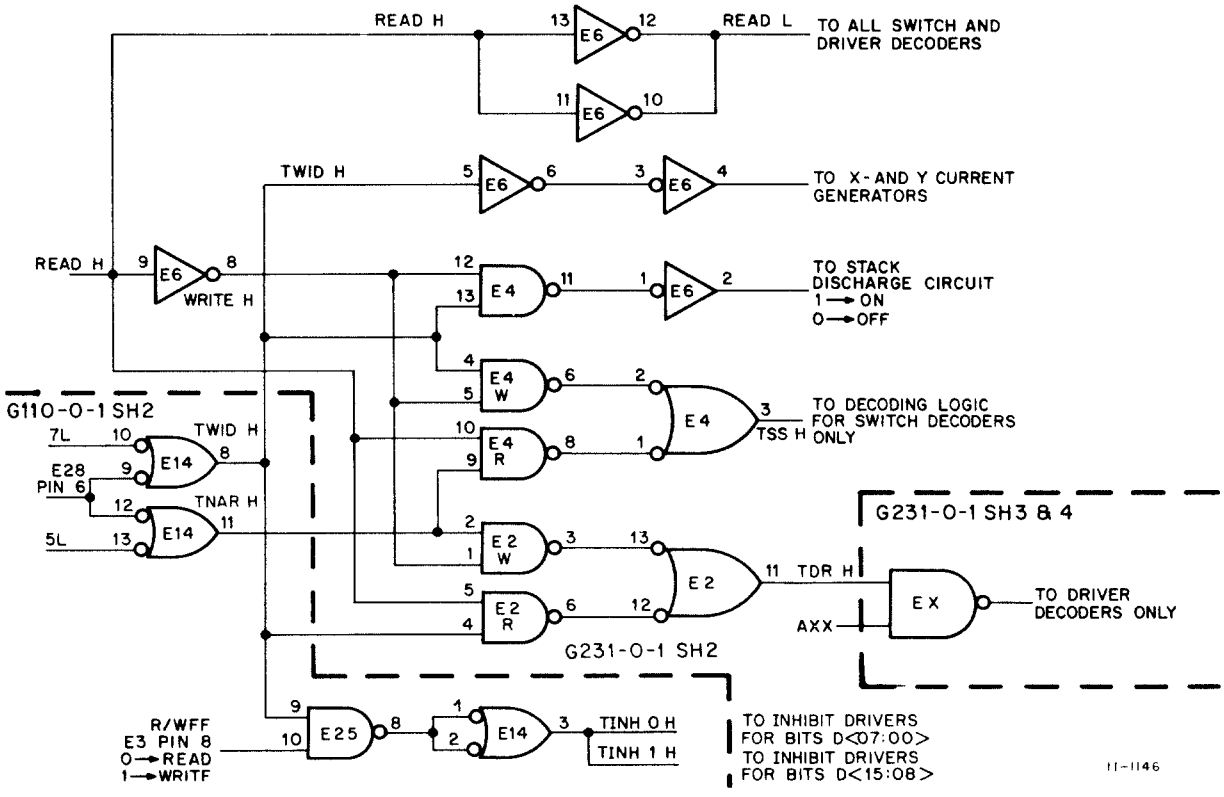


Figure 12-21 TWID H and TNAR H Control Logic

Signal TWID H is ANDed with the 0-output (pin 8) of R/W flip-flop E3 at pins 9 and 10 of gate E25. With TWID H high, E25 is asserted only when E3, pin 8 is high; this occurs only during a write operation. The output (pin 8) of E25 is inverted by E14 to procure TINH 0 H and TINH 1 H. The output of E14 is physically divided into two paths: TINH 0 H activates the inhibit drivers for bits D (07:00), and TINH 1 H activates the inhibit drivers for bits D (15:08). These signals do not leave the control module because the inhibit drivers are also on this module.

Signals TWID H and TNAR H leave the control module (G110) and are sent to the drive module (G231). TWID H is sent to pin 4 of E2R, and TNAR H is sent to pin 2 of E2W. Gates E2 and E4 are marked W and R in Figure 12-21 to show their association with write or read operations. READ H is sent from the 1-output (pin 9) of R/W flip-flop E3 on the control module to pin 9 of inverter E6 on the driver module. READ H is high during a read operation and low during a write operation. Assume that a read operation is selected. READ H is high at pin 9 of E6 and is sent to pin 5 of E2R to be ANDed with TWID H. This gate is asserted and its low output is sent to pin 12 of negative-input NOR gate E2, which inverts it to produce TDR H. This signal is a decoding input for the memory read/write drivers only. Gate E2W is not asserted because WRITE H, which is the inversion of READ H, is low. Therefore, TWID H controls decoding signal TDR H during a read operation. During a write operation, READ H is low and WRITE H is high. Signal TDR H is asserted via the output of gate E2W, using the ANDing of WRITE H and TNAR H. Decoding signal TDR H is controlled by TNAR H during a write operation.

A similar logic network is used to control signal TSS H, which enables six decoding signals that are in turn used to control memory read/write switches only. When gates E4W, E4R, and E4 are used, TSS H is generated at the output (pin 3) of E4. During a read operation, TNAR H controls enabling signal TSS H; signal TWID H controls TSS H during a write operation.

TWID H controls the operation of the X- and Y-current generators. During read and write operations, when TWID H is high, the signal is double inverted by two E6 inverters to turn both current generators on.

The TWID H signal also controls the operation of the stack discharge circuit. It is ANDed with WRITE H at pins 13 and 12 of NAND gate E4. The output (pin 11) of E4 is inverted by E6 to control the stack discharge circuit. This circuit is considered to be turned on when the output (pin 2) of E6 is high. This occurs during a write operation when TWID H and WRITE H are both high.

Although not part of the timing circuit, Figure 12-21 shows READ H inverted by two E6 inverters to become READ L, which is a decoding input to all 8251 decoders for the memory switches and drivers. During a read operation, READ H is high and READ L is low, which selects only read switches and drivers; conversely, during a write operation, READ L is high, which selects only write switches and drivers (Paragraph 12.4.3.2).

MSEL RESET

The memory select (MSEL) flip-flop E2 is cleared (reset) at the end of a read operation in DATIP mode and at the end of a write operation in all other modes (DATI, DATO, and DATOB) by signal MSEL RESET L. The MSEL RESET L signal is generated at the output (pin 8) of gate E16 (a type 74H53 2-2-2-3 input AND-OR-invert gate). Three of its four AND inputs are used to facilitate the various methods used in generating MSEL RESET L (Figure 12-22).

When the system is turned on, the processor asserts BUS INIT L on the Unibus. The output of bus receiver E7 is high; this high output is sent to pins 9 and 10 of E16 to generate MSEL RESET L at its output (pin 8). The MSEL RESET L signal is passed through a 100-ns delay line (DL3) to the clear input (pin 1) of MSEL flip-flop E2, which directly clears (resets) it. All memory operations start with E2 cleared; however, this flip-flop is set approximately 75 ns after the processor asserts BUS MSYN L. It remains set until it is cleared by one of the following operations.

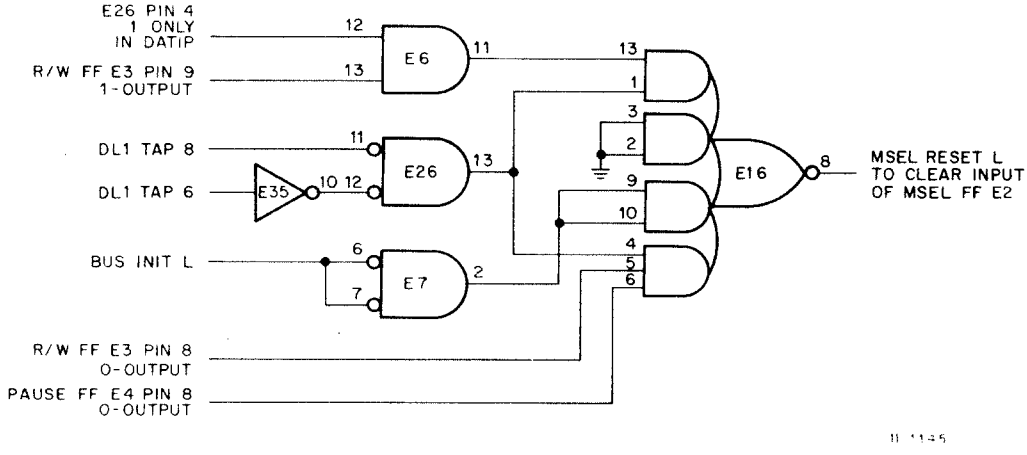


Figure 12-22 Generation of MSEL RESET L

In the DATIP mode, pin 12 of AND gate E6 is high; in all other modes, it is low, disqualifying E6. A read operation is performed in DATIP, and R/W flip-flop E3 is set. The 1-output of E3 is sent to pin 13 of E6. At this time, pin 13 is high and a high is generated at the output (pin 11) of E6. This AND input is qualified when pin 1 is also high, which occurs when DL1 tap 6 is high and DL1 tap 8 is low. Tap 6H is inverted by E35 and sent to pin 12 of E26. Tap 8L is sent directly to the other input (pin 11) and the gate is asserted; this gate sends a high to pin 1 of E16, which generates MSEL RESET L at the output (pin 8) of E16. This low signal clears MSEL flip-flop E2 at the end of the read operation (timed by 6H and 8L).

In all other modes (DATI, DATO, and DATOB), signal MSEL RESET L is generated at the end of the write operation (except DATO or DATOB following a DATIP). The R/W flip-flop is set, making its 0-output (pin 8) low, which disqualifies the 3-input (pin 4, 5, and 6) AND gate in E16.

Taps 6H and 8L cannot qualify this AND input or the other AND input (pins 1 and 13) because the memory is not in the DATIP mode. Therefore, the read operation is completed and MSEL RESET L is not generated. The write operation is now started and the R/W flip-flop is cleared, which puts a high on input 5 of E16. Input 6 is high because the PAUSE flip-flop is reset (pin 8 is a 1). Now, when tap 6 is high and tap 8 is low, input 4 of E16 is high. This generates signal MSEL RESET L to clear MSEL flip-flop E2 at the end of the write operation. This circuit performs the function of a memory bus flip-flop.

R/W RESET

The timing for the generation of the signal to clear (reset) R/W flip-flop E3 is obtained from taps 8 and 9 of DL1. Tap 9 is sent directly to pin 8 of E26. Tap 8 is inverted by E35 and sent to pin 9 of E26. When tap 9 is low and tap 8 is high, E26 is asserted (output pin 10 is high). This signal is sometimes called R/W RESET H. It is ANDed with READ H at pins 2 and 1 of NAND gate E18 to generate R/W RESET L. When this signal is a low, it directly resets R/W flip-flop E3 via its clear input (pin 13). READ H is high when the R/W flip-flop is set because it comes from the 1-output (pin 9). The remainder of the control signals shown in Figure 12-20 are discussed in the circuit descriptions contained in Paragraph 12.9.2, Slave Synchronization Circuit; Paragraph 12.9.3, Pause/Write Restart Circuit; and Paragraph 12.9.4, Strobe Generating Circuit.

12.9.2 Slave Synchronization (SSYN) Circuit

Slave synchronization (SSYN) is the response of the slave device to the master, usually a response to master synchronization (MSYN). The master places address information, mode control information, and data (if a DATO or DATOB is selected) on the Unibus. It then asserts BUS MSYN L but only if BUS SSYN L from the slave is cleared, which indicates that the slave can participate in a bus transaction. The slave asserts BUS SSYN L when it has data to send (DATI or DATIP) or when it has received data (DATO or DATOB). The master receives BUS SSYN L in both cases and clears BUS MSYN L. When the slave receives the cleared BUS MSYN L, it clears BUS SSYN L which frees the bus. This brief statement of the SSYN/MSYN interaction is necessary to understand the operation of the memory SSYN circuit. Details of the SSYN/MSYN interaction during all bus transactions can be found in the *PDP-11 Peripherals Handbook.* The SSYN circuit is shown in drawing G110-0-1, sheet 2; however, for clarity, only the SSYN circuit is shown in Figure 12-23 along with the appropriate timing diagram.

During a DATI or DATIP transaction, signal BUS SSYN L is asserted by the memory when the data is placed on the Unibus by the MDR. During a DATO or DATOB transaction, BUS SSYN L is asserted by the memory when it receives data from the Unibus.

At the start of each transaction, the master first places the memory address (device and word) and mode control information on the Unibus. (Data is included if the transaction is DATO or DATOB.) For a DATI or DATIP transaction, BUS C01 L is high at pin 10 of bus receiver E29. The output (pin 14) of E29 is low and is sent to the D-input (pin 6) of C01 latch E30 and to pin 5 of the E5 WRITE gate. Signal BUS MSYN L has not yet been asserted; thus, the output (pin 13) of bus receiver E23 is low. This signal is sent to pin 2 of NOR gate E26: the other input (pin 3) of this gate is always low because MSYN A L is normally not connected. The output (pin 1) of E26 is inverted by E15 to produce SSYN RESET L; this signal sets SSYN flip-flop E4 via its preset input (pin 4). The low 0-output (pin 6) is sent to both inputs of bus driver E5. The output of this gate is the slave synchronization signal (BUS SSYN L) and, at this point, it is not asserted.

As long as BUS MSYN L is not asserted, the SSYN flip-flop is preset. The master now asserts BUS MSYN L, which in turn disables the preset signal to the SSYN flip-flop (SSYN RESET L is high). Clock signal CLK 1 H is generated and clocks C01 latch E30. Latch E30 is reset and its high 0-output (pin 11) is sent to pin 10 of the E5 READ gate in the wired-AND. The wired-AND output CLK SSYN is high, and it remains high as long as both E5 NAND gate outputs are high; this occurs when at least one input of each gate is low. The output of E5 WRITE remains high because input pin 5 is held low by the output of C01 receiver E29. The output of this gate is not changed when the CLK 2 H pulse appears at pin 4. The output of E5 READ remains high until STROBE H goes low again; the wired-AND output is high again. This positive transition clocks the SSYN flip-flop, which now resets because its D-input is tied to ground (low). The high 0-output (pin 6) of the SSYN flip-flop asserts BUS SSYN L at the output (pin 3) of bus driver E5. The master receives the asserted BUS SSYN L signal and clears BUS MSYN L. The memory receives the cleared BUS MSYN L from the master at bus receiver E23 and generates signal SSYN RESET L via gates E26 and E15 to set the SSYN flip-flop. The memory is now ready for the next transaction.

For a DATO or DATOB, the sequence is the same except that BUS C01 L is low at pin 10 of bus receiver E29. This conditions the wired-AND so that the output of E5 READ remains high. In this case, the CLK 2 H pulse generates the CLK SSYN pulse that clocks the SSYN flip-flop via E5 WRITE.

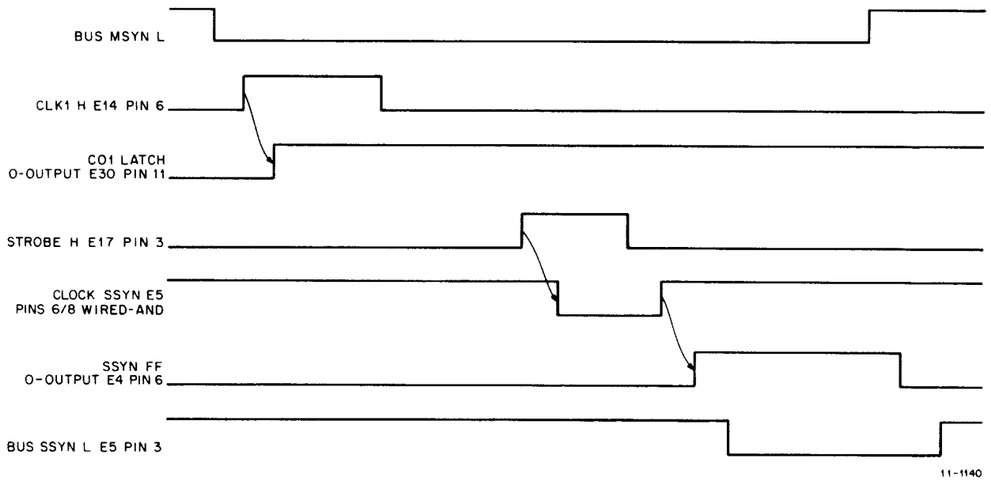
12.9.3 Pause/Write Restart Circuit

The PAUSE flip-flop is used to inhibit the restore (write) operation during a DATIP transaction. This transaction is useful when there is no need to restore data after reading because the location is to have new data written into it. By eliminating the restore operation, memory cycle time is decreased by approximately 50 percent. A DATIP must always be followed by a DATO or DATOB. In this case, the DATO or DATOB is shortened by eliminating the clear (read) operation that is normally performed prior to the restore (write) operation. The location has been cleared previously by the DATIP; consequently, the DATO or DATOB need only perform the restore (write) operation. The pause/write restart circuit is shown in drawing G110-0-1, sheet 2; however, for clarity, only the pause/write restart circuit is shown in Figure 12-24.

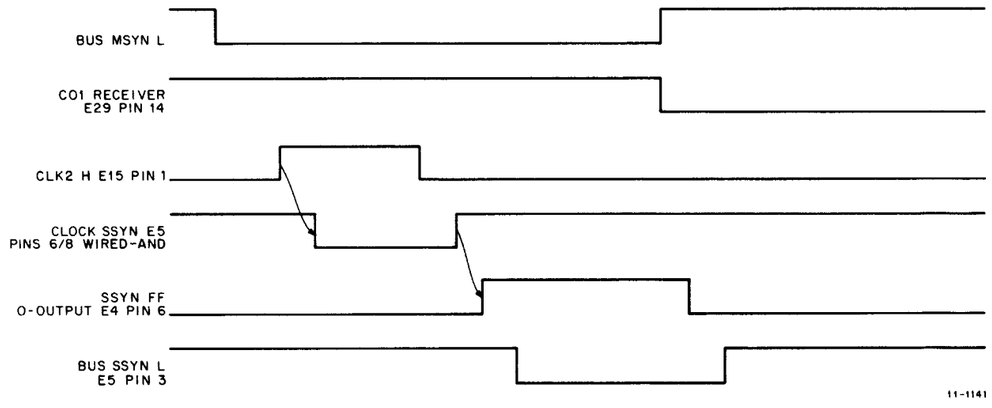
At the start of all bus transactions, the PAUSE flip-flop is reset; it remains reset throughout the bus transactions except during a DATIP, in which case it is set during the read operation. The PAUSE flip-flop is clocked by the reset 0-output (pin 6) of the SSYN flip-flop. The state (set or reset) of the PAUSE flip-flop is determined by its D-input (pin 12): the D-input is high to set and low to reset. The state of the D-input is controlled by Unibus mode control bits C01 and C00. (Only the mode control representing a DATIP provides a high to the D-input of the PAUSE flip-flop.) During a DATIP, C01 is high and C00 is low at bus receivers E29, pin 10 and E29, pin 7. These signals are inverted by the bus receivers and applied to the D-input of the C01 and C00 latches: C00 latch E30, pin 3 is high, and C01 latch E30, pin 6 is low. When the latches are clocked by the CLK 1 H signal, latch C01 is reset and C00 is set. This action puts a low on each input of negative input AND gate E26, which generates a high output. This high output is the D-input to the PAUSE flip-flop. The PAUSE flip-flop is now conditioned to set when it is clocked.

Returning to the start of the DATIP operation, the PAUSE flip-flop is reset. Its D-input is conditioned (D is high) but the PAUSE flip-flop has not been clocked; thus, its 0-output (pin 8) is high. This high output goes to the D-input of the Read/Write flip-flop (R/W E3); this flip-flop is clocked early in the sequence by CLK 1 H. The R/W flip-flop is then set which permits a read operation. The low 0-output (pin 8) of the R/W flip-flop is sent to pin 4 of E17. The other input (pin 5) of E17 comes from the 0-output (pin 8) of the PAUSE flip-flop, and it is a high at this time. The output of E17 is a high and is inverted by E15, which puts a low on the clear input of the Write Restart flip-flop (WRRS E2). The output of E15 also goes to input 2 of E25. The WRRS flip-flop is cleared (reset) and its high 0-output (pin 8) is sent to the other input (pin 1) of E25. The output of E25 is the WRITE RESTART L signal. This signal is produced to trigger the timing circuit and to initiate a write operation. Signal WRITE RESTART L is now high, its proper state when a read operation is being performed.

At the end of the read operation, the SSYN flip-flop is clocked which resets it. The positive transition at its 0-output (pin 6) clocks the PAUSE flip-flop, which sets the SSYN flip-flop and puts a low on pin 5 of E17. The timing circuit clears (resets) the R/W flip-flop, which in turn puts a high on pin 4 of E17. The output of E17 remains high, inhibiting the WRITE RESTART L signal and preventing the initiation of a write operation.



Timing Diagram for SSYN Circuit During DATI and DATIP



Timing Diagram for SSYN Circuit During DATO and DATOB

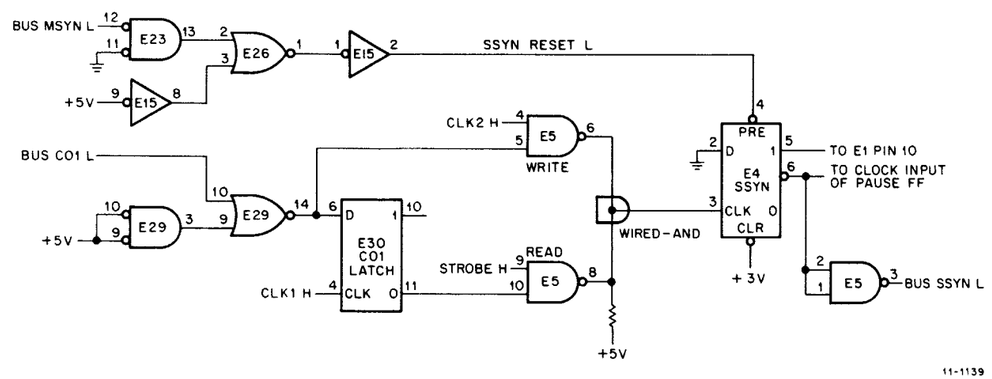


Figure 12-23 Slave Sync (SSYN) Circuit

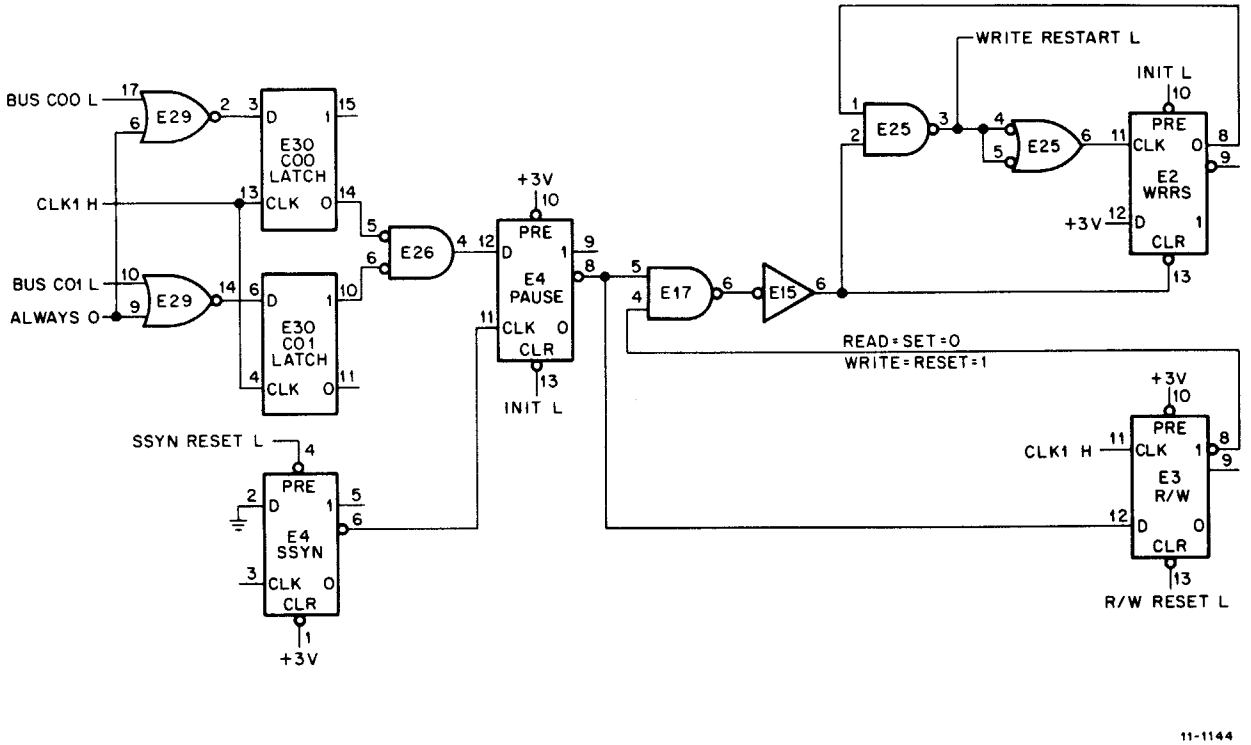


Figure 12-24 Pause/Write Restart Circuit

For any transaction other than DATIP (DATI, DATO, or DATOB), the PAUSE flip-flop is not set when it is clocked because its D-input is low. It remains reset which keeps a high on pin 5 of E17.

When the R/W flip-flop is cleared, it puts a high on pin 4 of E17. The low output of E17 is now inverted by E15 and sent to pin 2 of E25. The WRRS flip-flop is reset so that pin 1 of E25 is also high. The output (pin 3) of E25 goes low, which generates WRITE RESTART L. This starts the formation of a low WRITE RESTART L pulse. This output is inverted by E25, pin 6 which clocks the WRRS flip-flop and sets it, because its D-input is connected to +3V. Pin 8 of the WRRS flip-flop now goes low, which is in turn fed to pin 1 of E25. Thus, the output of E25 becomes high again, which terminates the low WRITE RESTART L pulse. This pulse triggers the timing circuit and initiates a write operation.

For a DATO or DATOB following a DATIP, the PAUSE flip-flop is reset by the SSYN flip-flop, because the DATO or DATOB transaction started with the PAUSE flip-flop set previously by the DATIP.

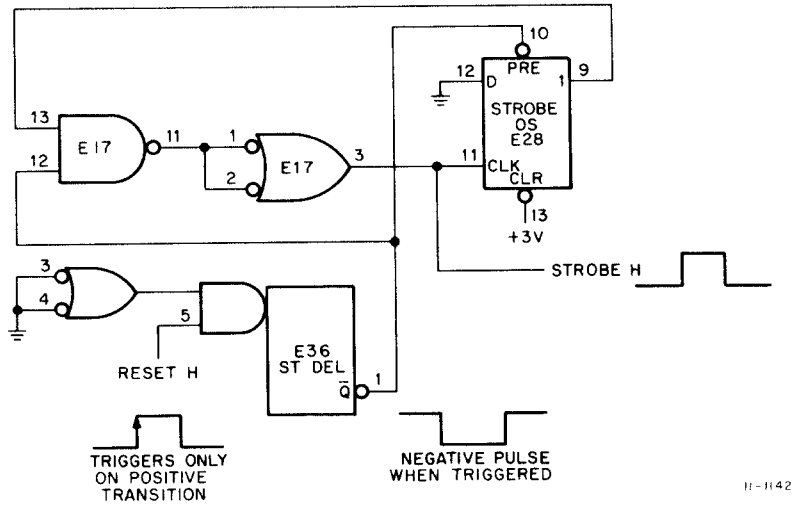
12.9.4 Strobe Generating Circuit

The strobe generating circuit produces a narrow positive pulse (STROBE H) during the read operation to enable the STROBE 0 H and STROBE 1 H signals for the sense amplifiers. The strobe generating circuit is shown in drawing G110-0-1, sheet 2; however, for clarity, only the strobe generating circuit is shown in Figure 12-25 along with an appropriate timing diagram.

During the read operation, the timing circuit generates a positive RESET H pulse. The RESET H pulse is sent to pin 5 of the strobe delay one-shot (ST DEL E36); this 74121 one-shot provides complementary outputs but only the Q (negative pulse) output (pin 1) is used. Pins 3 and 4 of the ST DEL one-shot are connected to ground so that it can be triggered by a positive-going edge at pin 5. Prior to receiving the triggering signal (RESET H), the strobe generating circuit is in the quiescent state. The STROBE 0S flip-flop E28 is in the reset state. (When the memory is

powered up, E28 is driven to the reset state by E36 if it did not come up reset randomly.) The low 1-output (pin 9) of E28 is sent to pin 13 of E17. The ST DEL one-shot is inhibited so that its $\overline{Q}$ output (pin 1) is high, which is sent to pin 12 of E17. The output (pin 11) of E17 is high and is inverted by the next E17 gate (pin 3). This is the STROBE H signal, and it is low at this time.

The timing circuit generates a positive RESET H pulse that is sent to pin 5 of E36. The positive edge of RESET H triggers E36, and its $\overline{Q}$ output (pin 1) goes to low. This is the start of a single negative pulse whose duration is determined by an external RC circuit connected to pins 10 and 11 of E36. The output of E36 directly sets STROBE E 0S flip-flop E28 via its preset input (pin 10). The 1-output (pin 9) of E28 goes high and is sent to pin 13 of E17. The other input to this gate (pin 12) is now low. E17, pin 11 is high and is inverted so that E17, pin 3 is still low (no strobe pulse yet). When E36 times out, its output (pin 1) goes high again. Pins 12 and 13 of E17 are now both high, and the output (pin 11) of E17 is low. This signal is inverted and E17, pin 3 is high. This is the beginning of the STROBE H pulse. The positive transition of E17, pin 3 also clocks flip-flop E28. E28 is reset because its D-input is connected to ground (low); pin 9 of E28 is now low. It is fed back to pin 13 of E17, which makes E17, pin 3 low again. This terminates the positive STROBE H pulse. The circuit is back to its quiescent state where it remains until another RESET H pulse comes along to trigger ST DEL one-shot E36.



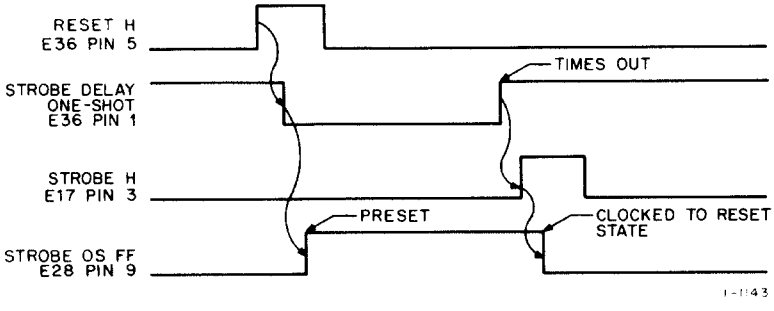


Figure 12-25 Strobe Generating Circuit and Timing Diagram for STROBE H

12.9.5 Data In (DATI) Operation

In the discussion of the DATI operation (as well as the DATIP, DATO, and DATOB operations) signals are not traced through circuit components; rather, various events are integrated to describe a complete memory operating cycle. All the circuits involved have been discussed in detail in the preceding paragraphs of this chapter. Refer to engineering logic drawings G110-0-1, sheets 2, 3, and 4; G231-0-1, sheets 2, 3, and 4; MM11-L-3 (timing diagram); and Figure 12-26, which is a flow chart for memory operation.

In a DATI operation, the master requests that a selected memory location be read and the information transferred to the master via the Unibus. The readout is destructive because the read operation forces all cores in the selected location to 0. However, during readout, the information is temporarily stored in the MDR and is automatically restored to the selected location by a write operation that immediately follows the read operation.

At the start of the DATI, MSEL flip-flop is reset, DEL flip-flop is reset, R/W flip-flop is reset, PAUSE flip-flop is reset, and SSYN flip-flop is set. The address lines and mode control lines (C01 and C00) are decoded. The master asserts the BUS MSYN L signal and the cycle begins. Signal CLK 1 H is generated, the DEL flip-flop is set, and the R/W flip-flop is set. Setting the DEL flip-flop initiates the timing chain via delay line DL1. The timing chain generates TWID H and TNAR H. At the same time, CLK 2 H is generated and it presets the MSEL flip-flop, which prevents the start of another cycle until it is reset. Signal READ H from the R/W flip-flop and signals TNAR H and TWID H go to the driver module to select the appropriate read drivers and switches, turn on the X- and Y-current generators, and control the stack discharge circuit. As a result of these signals, the X- and Y-half currents are directed to the selected memory location, and all 16 cores (one per bit plane) are set to 0. Just prior to this event, the timing chain generates RESET 0 L and RESET 1 L; these signals clear the MDR. The timing chain then generates STROBE H, which asserts STROBE 0 H and STROBE 1 H; these signals are sent to the sense amplifiers. The strobe pulses are timed to arrive at the same time as the pulses induced in the sense/inhibit line. If a selected core is a 1, a pulse is induced in the sense/inhibit line that exceeds the sense amplifier threshold and produces an amplified positive pulse. This output is inverted and presets its associated MDR flip-flop and a 1 is stored in the flip-flop. Signal STROBE H also clocks the SSYN flip-flop which resets. The SSYN flip-flop output asserts DATA OUT H and BUS SSYN L. Signal DATA OUT H gates the output of the MDR to the Unibus. BUS SSYN L is a Unibus signal that informs the master that the memory has read the selected location and placed the data on the Unibus. The master takes the data and clears BUS MSYN L,which in turn generates SSYN RESET L to set the SSYN flip-flop. BUS SSYN L is cleared to indicate that the Unibus is free; however, another bus transaction cannot be initiated even if the master asserts BUS MSYN L because the lockout feature of the MSEL flip-flop is still set. Prior to the assertion of BUS SSYN L, the timing chain generates DELAY FF RESET L, which resets the DEL flip-flop and allows the TNAR H and TWID H pulses to terminate as a function of taps 5 and 7 of the delay line. The timing chain also generates R/W RESET L, which resets the R/W flip-flop.

The memory now enters the write (or restore) cycle. With the R/W flip-flop and PAUSE flip-flop both reset, the pause/write restart circuit generates the WRITE RESTART L signal, which initiates another timing cycle by setting the DEL flip-flop.

The timing chain generates TWID H and TNAR H. These signals, plus a low READ H signal from the R/W flip-flop, go to the driver module to select the appropriate write drivers and switches; turn on the X- and Y-current generators; and control the stack discharge circuit. In addition, TWID H and an output from the R/W flip-flop are ANDed to generate TINH 0 H and TINH 1 H. These signals control the operation of the inhibit drivers. Signals TINH 0 H and TINH 1 H are ANDed with the outputs of the MDR flip-flops. If a 1 is stored in the MDR flip-flop, the associated inhibit driver is not turned on and a 1 is written into this bit of the selected memory location. If a 0 is stored in the MDR flip-flop, the associated inhibit driver is turned on and produces a current that opposes the Y-line current and prevents a 1 from being written into this bit. The timing chain generates DELAY FF RESET L, which resets the DEL flip-flop and allows TNAR H, TWID H, and the inhibit pulses (TINH 0 H and TINH 1 H) to terminate. The timing chain also generates MSEL RESET L, which resets the MSEL flip-flop.

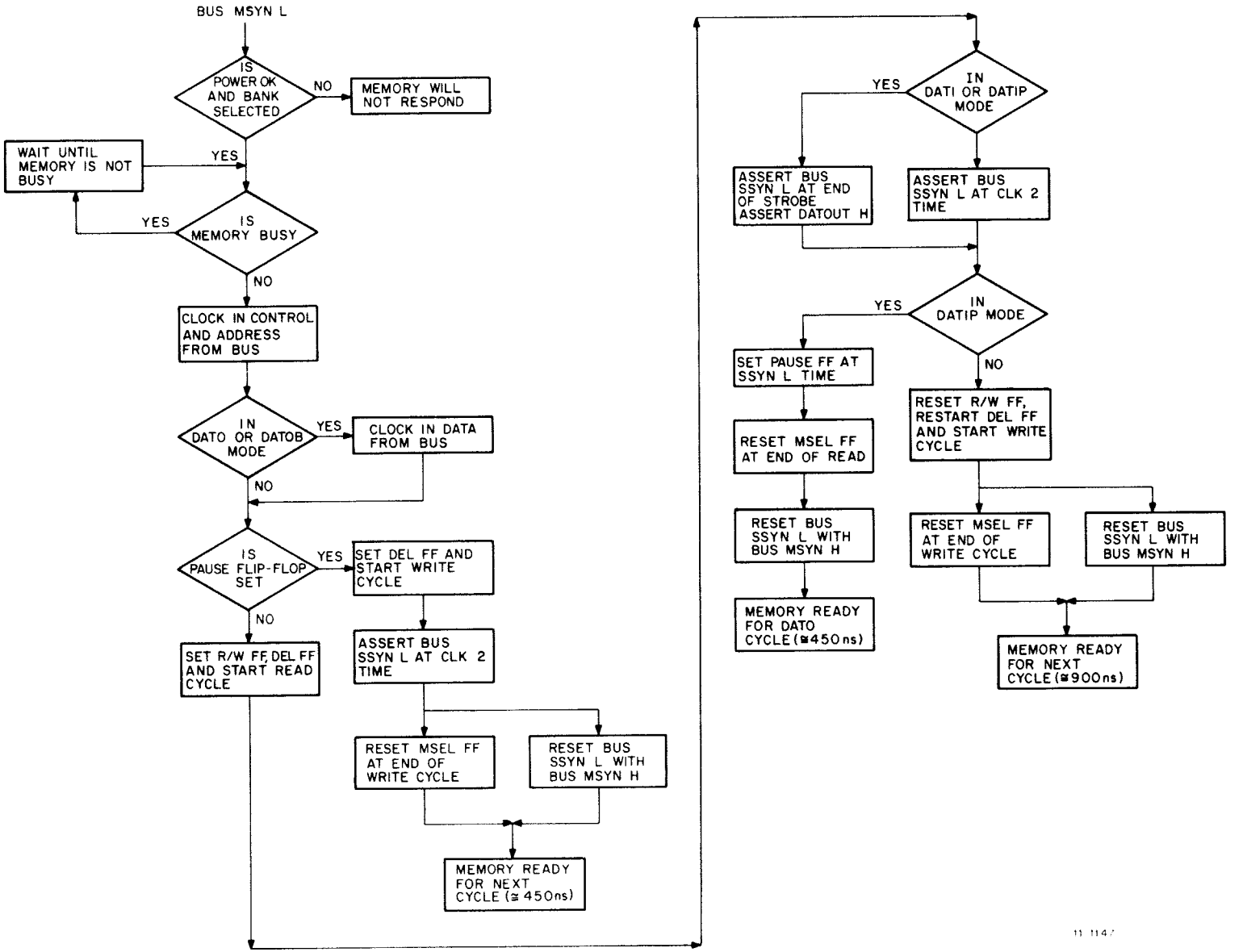


Figure 12-26 Flow Chart For Memory Operation

12.9.6 Data In Pause (DATIP) Operation

In a DATIP operation, the master requests that a selected memory location be read and the information transferred to the master via the Unibus. However, unlike the DATI, this information is not to be restored after reading; this location is to have new information written into it. The DATIP performs only a read operation; the write operation is inhibited. A DATIP must always be followed by a write operation (either DATO or DATOB).

The read operation of a DATIP is identical to that of a DATI (Paragraph 12.9.5) until the time the SSYN flip-flop is reset (clocked by STROBE H). At this time, the SSYN flip-flop output clocks the PAUSE flip-flop, which sets it because its D-input is a 1 (only during DATIP due to the state of mode control bits C01 and C00). The timing chain generates R/W RESET L which resets the R/W flip-flop. The outputs of the PAUSE flip-flop and R/W flip-flop prevent the pause/write restart circuit from generating WRITE RESTART L. With this signal inhibited, the write operation is not produced. The timing chain generates DELAY FF RESET L, which resets the DEL flip-flop and terminates TNAR H and TWID H. The timing chain also generates MSEL RESET L, which resets the MSEL flip-flop.

The memory is now ready to accept another request from the master. The next operation must be a DATO or DATOB. Normally, a DATO or DATOB starts with a read operation to set all selected cores to zero (clear) before writing new information into them. A DATO or DATOB following a DATIP has this initial clear operation eliminated because the cores have been cleared by the previous DATIP operation.

The DATO or DATOB following a DATIP starts when the master asserts BUS MSYN L. Pulse CLK 1 is generated but it does not set the R/W flip-flop because the PAUSE flip-flop is set. The master places the information to be written on the Unibus where it is picked off by bus receivers and sent to the D-input of the MDR flip-flops. Decoding the mode control bits (C01 and C00) for a DATO or DATOB generates LOAD 0 H and LOAD 1 H, which clock the MDR flip-flops. The outputs of the MDR flip-flops are gated with TINH 0 H and TINH 1 H to control the associated inhibit drivers to write 1s or 0s into the selected memory location. As in the write operation of a DATI, the timing chain generates TWID H and TNAR H which select the appropriate write drivers and switches; turn on the X- and Y-current generators; and control the stack discharge circuit. They also generate inhibit driver control signals TINH 0 H and TINH 1 H. Signal CLK 2 H clocks the SSYN flip-flop (resets it), which asserts BUS SSYN L to tell the master that the data has been taken from the Unibus. When the master clears BUS MSYN L, the SSYN flip-flop is reset, which in turn resets the PAUSE flip-flop. At the end of the write operation, the timing chain generates DELAY FF RESET L and MSEL RESET L to restore the control signals to their original states.

12.9.7 Data Out (DATO) Operation

In a DATO operation, the master sends a 16-bit word to be written into the selected memory location. The transaction starts with a read (clear) operation to set the selected cores to 0 before writing new data into them. The standard DATO consists of a read operation followed by a write operation. (As described in Paragraph 12.9.6, a DATO following a DATIP does not perform the read operation.)

The read operation of a DATO is similar to a read operation of a DATI except that no RESET 0 L, RESET 1 L, STROBE 0 H, and STROBE 1 H pulses are generated. The MDR is not cleared and the sense amplifiers are not strobed. This read operation is required only to clear the memory location by setting all the selected cores to 0; it is not necessary to readout and store the information in the MDR. The information on the Unibus data lines is sent to the inputs of the MDR flip-flops. Decoding the mode control bits (C01 and C00) generates LOAD 0 H and LOAD 1 H, which clock the MDR flip-flops. The MDR outputs (16 bits) are gated with TINH 0 H and TINH 1 H to control the associated inhibit drivers. The timing chain generates the other control signals that provide the selection of the appropriate write drivers and switches and a write operation is initiated. This write operation is the same as that described in Paragraph 12.9.6 for a DATO following a DATIP.

12.9.8 Data Out Byte (DATOB) Operation

In a DATOB operation, the master sends a byte (8 bits) to be written into the selected memory location. A high byte [bits D (15:08)] or a low byte [bits D (07:00)] can be selected. Byte selection is made by the state of address bit A00. A DATOB is the same as a DATO except that the selected and non-selected bits are handled differently.

Assume that the low byte [bits D (07:00)] is selected (A00 = 0). Neither RESET 0 L or STROBE 0 H are generated for the selected byte because new data is to be written into bits D (07:00) (low byte). The LOAD 0 H signal is generated so that the data on Unibus bits D (07:00) can be written into the selected byte location.

The non-selected byte [bits D (15:08)] is to be restored so that RESET 1 L and STROBE 1 H are generated. These signals strobe the byte into the MDR for restoration during the write operation. Restoration is necessary because this byte does not receive new data. The LOAD 1 H signal is not generated; therefore, any data on Unibus bits D (15:08) has no effect on the non-selected byte.

When the DATOB is complete, the selected byte contains new data and the non-selected byte remains unchanged. A DATOB operation following a DATIP is the same, except that the read portion is eliminated.

CHAPTER 13
MEMORY MAINTENANCE

13.1 INTRODUCTION

This chapter provides the preventive and corrective maintenance procedures for the MM11-K and L memories. The user should have a thorough understanding of the normal operation of the memory (Chapter 12). This knowledge plus the maintenance information will aid the user in isolating and correcting malfunctions.

13.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks performed at intervals to detect conditions that could lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance items.

a. Visual inspection of modules for broken wired, connectors, or other obvious defects.
b. +5V and -15V checks: both must be within ±3%.
c. X- and Y-current generator check (Paragraph 13.2.2).

Two pieces of test equipment are recommended for checking and troubleshooting the memory: Tektronix 453 Dual Trace Oscilloscope or equivalent, and Honeywell 33R Digital Voltmeter or equivalent with 0.5 percent accuracy.

13.2.1 Initial Procedures

Before attempting to check, adjust, or troubleshoot the memory, perform the following steps.

NOTE
All tests and adjustments must be performed in an ambient temperature range of 20°C to 30°C (68°F to 86°F).

1. Verify that all modules are properly and securely installed.

CAUTION
Ensure that all power is off before installing or removing modules.

2. Visually check modules and backplane for broken wires, connectors, or other obvious defects.

3. Verify that power buses are not shorted together.

4. Turn on primary power and check that both the -15V and +5V power are present and within tolerances (±3%).

5. Start the system. The memory should operate without errors. If not, check the output of the current generator (Paragraph 13.2.2). If the memory still does not operate properly, a malfunction has occurred. Proceed with corrective maintenance (Paragraph 13.3).

13.2.2 Checking Output of Current Generators

The amplitude of the current pulse from each current generator (X and Y) is factory set at 410±5 mA. It is not adjustable in the field.

The X- and Y-current generators are located on the G231 Driver Module. Each output has a current loop on its output line for attaching a test probe. Loop J5 is for the Y-generator and loop J6 is for the X-generator (drawing G231-0-1, sheet 2). The amplitude of each READ current pulse should be 410±5 mA. At the time of measurement, -15V and +5V power must be within the specified tolerance of ±3 percent.

13.3 CORRECTIVE MAINTENANCE

This paragraph describes the method of interchanging the positions of the memory modules to gain access to test points. It also describes the strobe delay adjustment, which is a specific corrective maintenance procedure. Further, three aids are included for performing corrective maintenance: a troubleshooting chart and waveforms for the drive and sense/inhibit circuits.

13.3.1 Strobe Delay Check and Adjustment

CAUTION

Strobe delay is factory adjusted and should be adjusted only when one of the three modules is replaced. It is a critical adjustment and must be done carefully.

The strobe must be set while cycling worst-case noise test patterns (MAINDEC-11-DIGA). The proper setting is midway between the two end points where the memory starts to error as strobe time is moved from earliest to latest. As the strobe time is varied, allow adequate time to cycle completely through the worst-case noise test at each strobe position. Figure 13-1 shows the strobe pulse waveform and the READ pulse waveform and the points at which they are picked off for display. Strobe-adjusting potentiometer R120 is on the G110 module next to the large delay line (DL1) and is accessible without putting the module on the extender.

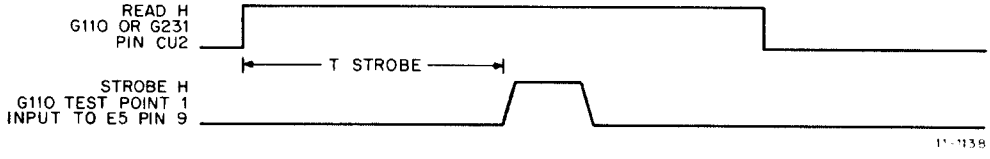


Figure 13-1 Strobe Pulse Waveform

13.3.2 Corrective Maintenance Aids

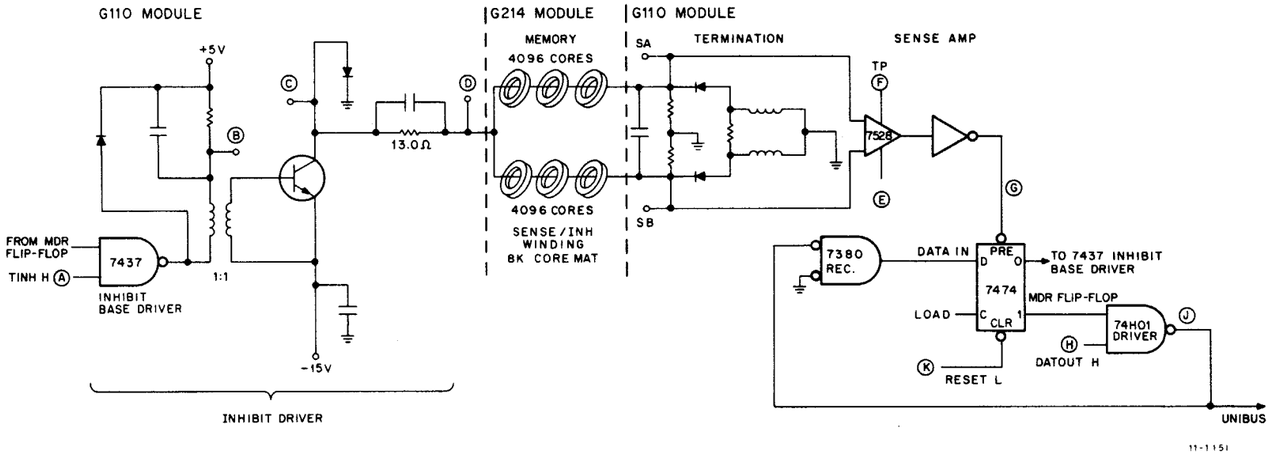
Figure 13-2 is a troubleshooting chart arranged as a two-axis grid that identifies faults versus cause location. Figure 13-3 illustrates the sense/inhibit waveforms, and Figure 13-4 illustrates the drive waveforms. Both figures include schematics to indicate the points in the circuit where the waveforms occur. In addition to nominal waveforms, dotted lines are used to indicate waveforms that appear if specific components are faulty.

Loc.	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	D C	C	C			S	S	S	S		D	D	D	D	D	D	D	D	D	D	D				
Possible Circuit / Failure Symptom	-5.1V	Device Selection or Jumpers	DELAY Flip-Flop or DELAY Line	MSEL Flip-Flop	SSYN Flip-Flop	PAUSE Flip-Flop	READ Flip-Flop	Write Restart Flip-Flop	STROBE H	RESET L	LOAD H	TINH H	DATA OUT H	INIT L Circuit	BALUN Transformer	Bus Receiver-Driver	Sense Amplifier or Terminator	Data Latch	Inhibit Driver	20-mV Threshold		Stack S/I Line	Stack X-Y Line	Stack Diode	Stack Resistor-Thermistor		X-Y Volt Reference Circuit	Stack Discharge Circuit	X I Generator	Y I Generator	YDR	YSS	XDR	XSS	TDR-TSSH	DC LO L Circuit	4K - 8K Jumper		Backplane	+5V	-15V
Memory Does Not Respond to MSYNL		X	X	X	X				X	X				X		X																				X		X	X	
Memory Hangs Bus					X																																				
DATO Fails											X			X		C00 C01		X																					X			
DATIP Fails						X								X		C00 C01																							X			
Many Bits Fail	X											X								+5 FA2																			X	X	
Picks Bits	Lo								Lo									X	X							Lo	X	Hi	Hi												Lo
Drops Bits	Hi								Hi																	Hi	X	Lo	Lo												
Byte Failures									X	X	X	X				A0																									
4 Bits Fail															X	X				X																					
2 Bits Fail																	X	X																							
1 Bit Fails																		X	X			X																	X		
Fails All Addresses	X	X											X												X		X	X	X	X					X	X			X	X	X
A1–A3 Common																						X	X					X													
A4–A6 Common																						X	X					X													
A7- A9 Common																						X	X						X	X											
A10–A13 Common																						X	X						X		X										
READ Waveforms Wrong																											X		X	X	X	X	X	X	X						
WRITE Waveforms Wrong												X															X		X	X	X	X	X	X	X						
No Inhibit												X							X			X																			X

Location { C = G110 Sense Control; S = Stack; D = G231 Driver }

X = Indicates Circuit Not Operable
Lo = Measured Parameter Too Low or Early
Hi = Measured Parameter Too High or Late

Figure 13-2 Troubleshooting Chart



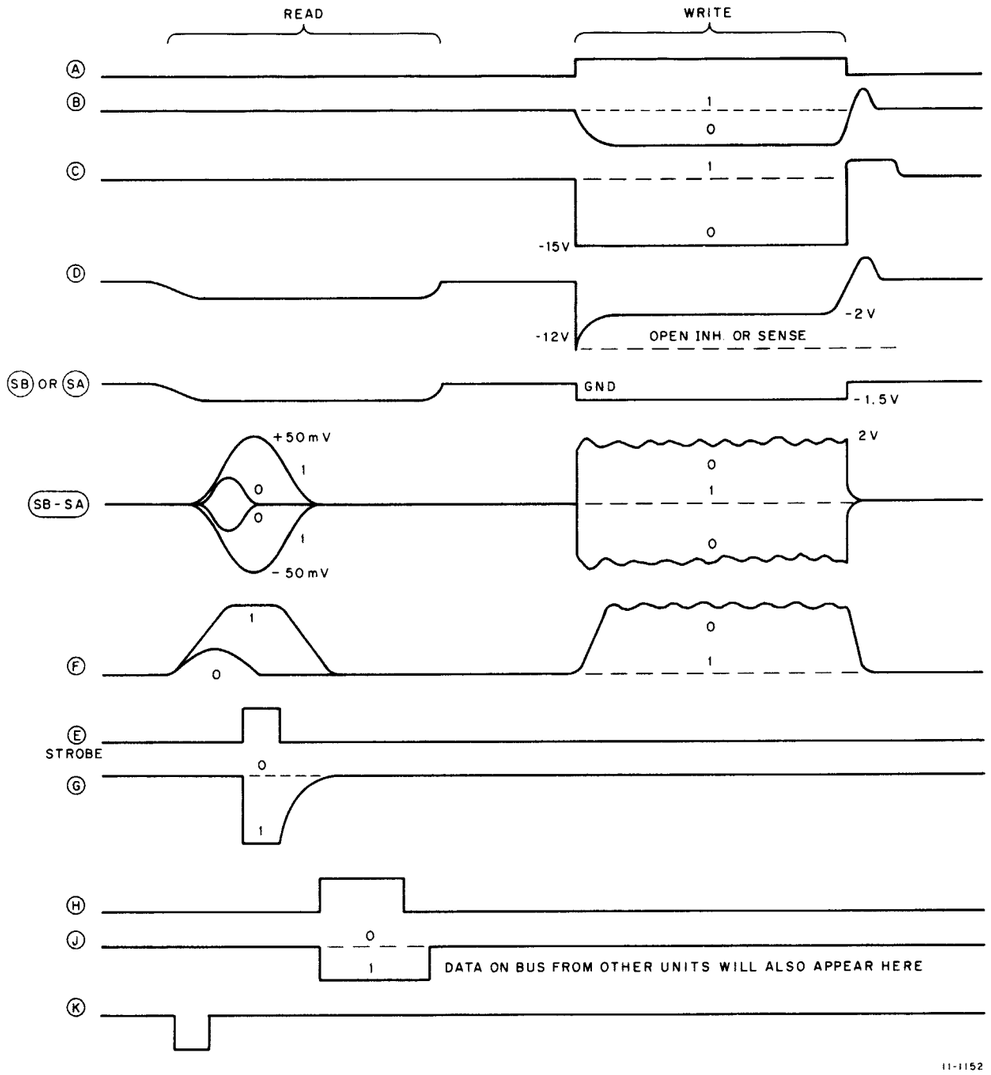
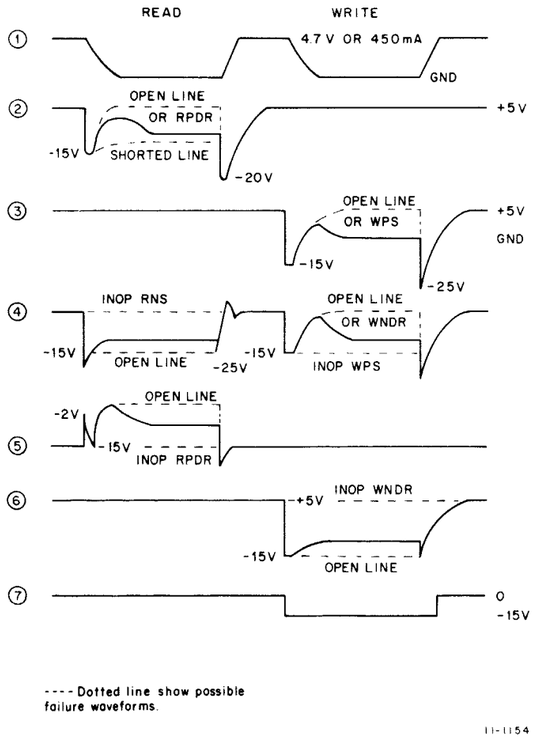


Figure 13-3 MM11-K Sense/Inhibit Waveforms



---- Dotted line show possible failure waveforms.

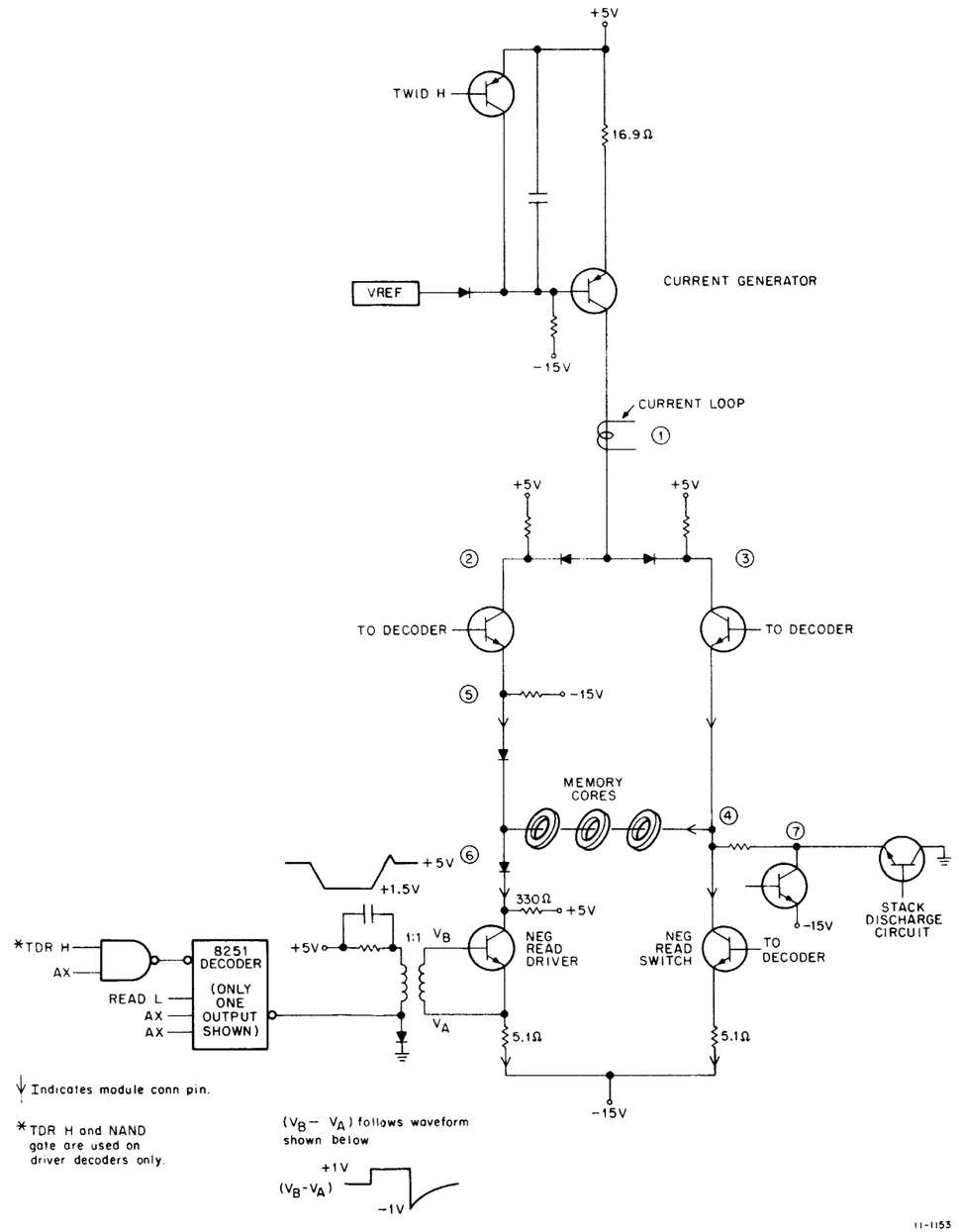


Figure 13-4 Drive Waveforms

13.4 PROGRAMMING TESTS

Certain DEC programs may be used to test various memory operations as an aid to troubleshooting. The purpose of each of these memory-related test programs, as well as the program abstract, is given in the following paragraphs. Each program contains instructions for use.

13.4.1 Address Test Up (MAINDEC-11-DIAA)

The purpose of the Address Test Up program is to demonstrate that the selected memory area is capable of basic read and write operations when address propagation is upward through memory. This test program writes the address of each memory location (within the test limits) into itself and then increments through memory until the address corresponding to the high limit is reached. After this location has been written, the memory enters the read cycle. The read cycle starts with the high limit location and reads and compares each word location, decrementing down to the low limit location. The program halts on an error.

The program ensures that all addresses are selectable and can also be used to isolate bad switches, wiring errors, or address selection errors. It will also find double selection errors when two bus addresses select the same core address.

13.4.2 Address Test Down (MAINDEC-11-DIBA)

The purpose of the Address Test Down program is to demonstrate that the selected memory area is capable of basic read and write operations when address propagation is downward through memory. It is a companion test to the Address Test Up program (Paragraph 13.4.1).

This test program writes the address of each location into itself, downward through memory. After writing down, the program reads and checks back up through the memory test area. The program halts on an error.

The Address Test Down program resides in the high portion of core memory. It does not check memory below address 100, as these locations are reserved for trap and vector locations. The program verifies that all modules can perform their basic functions, checks that all addresses are selectable, and can also be used to isolate faulty switches, wiring errors, or address selection errors.

13.4.3 No Dual Address Test (MAINDEC-11-DICA)

The purpose of the No Dual Address Test program is to check the unique selection of each memory address tested. This test is divided into two parts. The first portion of the test fills the test field with 1s and writes 0s into the first test location. This is followed by a read check from this location. The program then checks each field location to ensure there are no variations from the 1s configuration. Upon completion of this test, the test location pointer is incremented. The next location is then write/read exercised with 0s, and the test field rechecked for any change in content. When the selected test field has been tested in this mode, the program sets a flag and the second portion of the test is begun. The program fills the test field with 0s and the field is then tested with a write/read exercised with 1s.

This program checks for faulty switches or wiring errors, checks the complete address selection scheme, and checks all 16 bits in the data field for 1s and 0s operation.

13.4.4 Basic Memory Patterns Test (MAINDEC-11-DIDA)

The Basic Memory Patterns Test program has two main purposes:

a. Verify that the selected memory test field is capable of writing and reading fixed data patterns.

b. Verify that the memory plane is properly strung.

This test program writes a specific pattern throughout a given memory zone, then reads the pattern back and compares it with the original for correctness. If the pattern read fails to compare correctly with the original, the program initiates a call to the error subroutine. After completely checking the pattern, the program continues on to the next pattern test.

13.4.5 Worst-Case Noise Test (MAINDEC-11-DIGA)

The purpose of the Worst-Case Noise Test program is to generate the maximum possible amount of plane noise during execution of memory reference instructions to check system operation under worst-case conditions.

This test program is designed to produce the greatest amount of plane noise possible during memory read and write cycles. The noise parameters are affected by a number of factors. The noise generated is distributed across the core plane algebraically and adds to the normal dynamic noise present on the sense lines. This can cause misreading of data (within the plane) that is in the low (1) or high (0) category. The sense windings of most memories are such that worst-case patterns can be caused by alternately writing -1 and 0 data configurations throughout memory. Under these conditions, worst-case noise is generated by performing a read, write, complement operation at each location. The test is repeated after complementing all of the pattern data stored in the memory test zone; thus, all cores are tested for worst-case as both 1s and 0s. The pattern or its complement is written into the memory test zone as determined by the exclusive-OR between address bits 3 and 9.

The Worst-Case Noise Test program is divided into two parts. Part 1 is run first and, during this part of the program, a -1 configuration is written into all locations having an address with an exclusive-OR state between bits 3 and 9. All other locations are loaded with the 0 configuration. After the test zone has been loaded, the memory is rescanned. This time, each location is read, complemented, read, and complemented (RCRC). Any location detected as being disturbed by a previous RCRC operation is flagged as an error. Upon conclusion of the read scan loop, the program automatically switches to Part 2.

During Part 2 of the program, the data patterns stored in memory are complemented. In other words, 0 patterns are stored in locations having addresses with an exclusive-OR between bits 3 and 9. All other locations are loaded with the -1 configuration.

The exclusive-OR pattern distribution for Parts 1 and 2 is summarized for reference as follows:

Part 1
Exclusive-OR (3 and 9) = 1 pattern
No Exclusive-OR (3 and 9) = 0 pattern

Part 2
Exclusive-OR (3 and 9) = 0 pattern
No Exclusive-OR (3 and 9) = -1 pattern

After memory is loaded, it is scanned again with a read, complement, read, complement (RCRC) loop as previously described. Any location detected as being disturbed by a previous RCRC operation is flagged as an error.

Before writing or reading any location (in either part of the program), the program issues a call to subroutine XORCK (exclusive-OR check) that tests bits 3 and 9 and sets the XORFLG if the exclusive-OR condition is present.

Subroutine ERRORA is called for any location disturbed from the -1 configuration; subroutine ERRORB is called for any location disturbed from the 0 configuration.

The program prints out errors and repeats when complete without interruption. Upon completion, the program rings the teletype bell and then halts if switch 12 is present. A continue from the halt initiates another pass.

If the program indicates an error, use the troubleshooting chart as a guide to locate the fault.

PART 4

POWER SUPPLY

Part 4 provides specifications and a general physical description of the power supply. A detailed circuit description and maintenance information are also included. The chapters of Part 4 are:

CHAPTER 14
POWER SUPPLY GENERAL DESCRIPTION

14.1 INTRODUCTION

The power supply is a forced air-cooled unit that converts single-phase 115V or 230V nominal, 47-63 Hz line voltage to the three regulated output voltages required by the computer. The output voltages and their principal uses and characteristics are:

Voltage	Use	Characteristics
+15V	Communication Circuits	Series regulated and overcurrent protected.
+5V	IC Logic	Switching regulated and overvoltage and overcurrent protected.
-15V	Core Memory	Switching regulated and overvoltage and overcurrent protected.

The power supply is used in conjunction with the BC05HXX (115V) or BC05JXX (230V) Power Control Assemblies, which contain a line cord, circuit breaker, and RFI capacitors. Line cord length is specified in the part number; e.g., 115V, 6 feet is designated BC05H06.

The power circuitry also generates BUS AC LO L and DC LO L power fail early warning signals, and the LTC L real-time clock synchronizing signal.

A thermal control mounted on the heat sink will interrupt the ac input should the heat sink temperature become excessive due to fan failure or other cause.

14.2 PHYSICAL DESCRIPTION

The power supply comprises three major subassemblies and two cables: the power control unit, power chassis assembly, dc regulator module, dc cable, and ac cable.

14.2.1 Power Control Unit

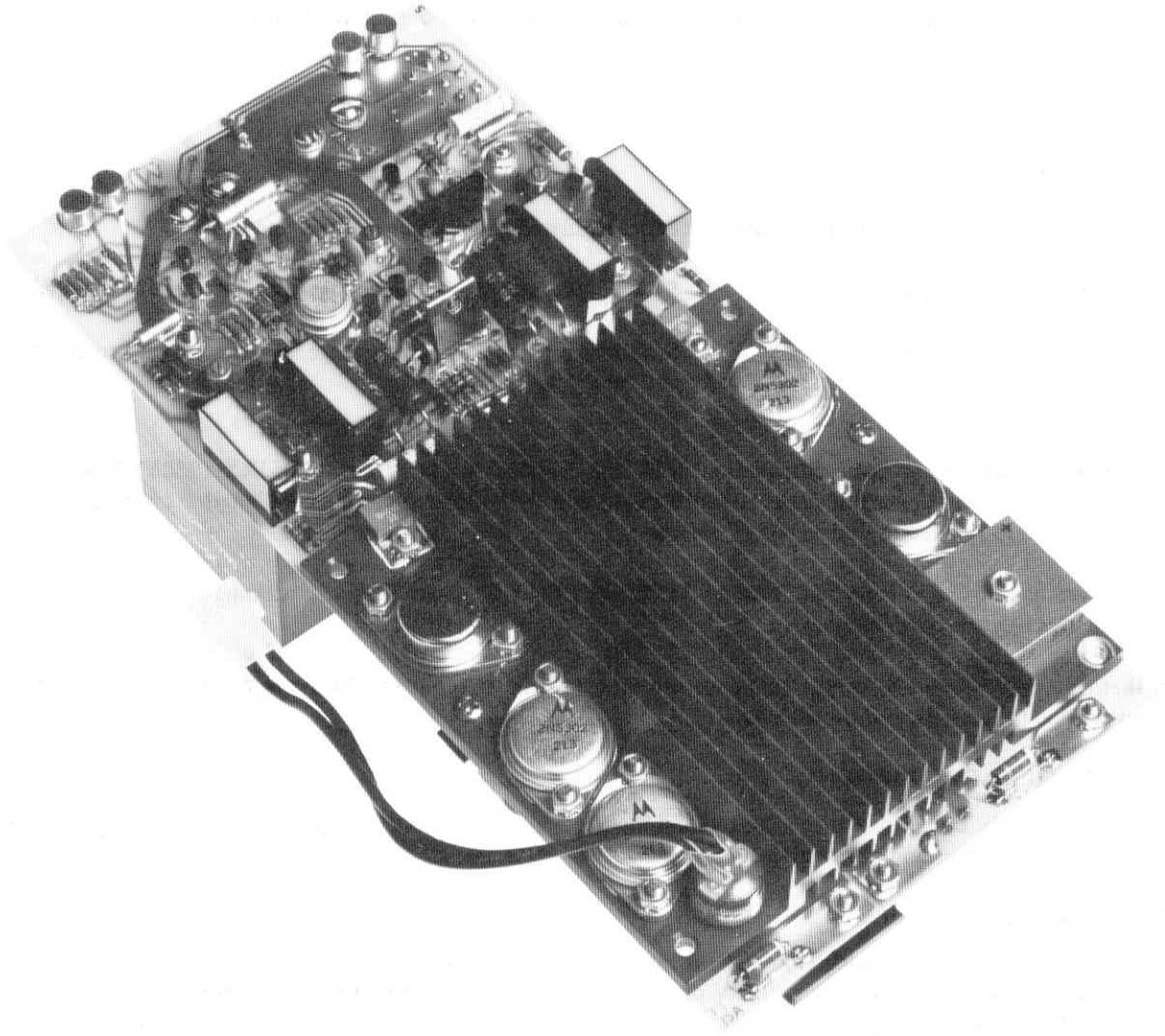
The power control unit (drawing H400-0-0) is mounted to the rear of the computer by two screws. It contains line cord, circuit breaker, RFI capacitors, 115V or 230V connections for the power supply transformer, and an output 6-socket Mate-N-Lok connector. Physically, it consists of a sheet metal bracket and a slide-on cover that is locked in place by one screw. A single pole thermal breaker and a line cord strain-relief grommet are mounted on the flange of the bracket, making the line cord and breaker reset button accessible on the rear of the computer.

A small printed circuit card is mounted directly to the breaker terminals. This card interconnects and mounts the RFI dual-disc ceramic capacitor, the output Mate-N-Lok connector and three fast-tabs for ac input and ground connections. A dual fast-tab is connected directly to the bracket. The black and white line cord wires are connected via fast-tab to the PC card; the green (ground) line cord wire is connected to the dual fast-tab, which in turn is connected to the third fast-tab on the PC card.

The 115V and 230V models differ in only two respects: breaker current rating and (printed circuit) jumpers for parallel or series connection of the power supply transformer primaries. Power control part numbers are: BC05HXX - 115V, 7A; and BC05JXX - 230V, 4A; where XX denotes line cord length; e.g., BC05H06 has a 6 foot line cord.

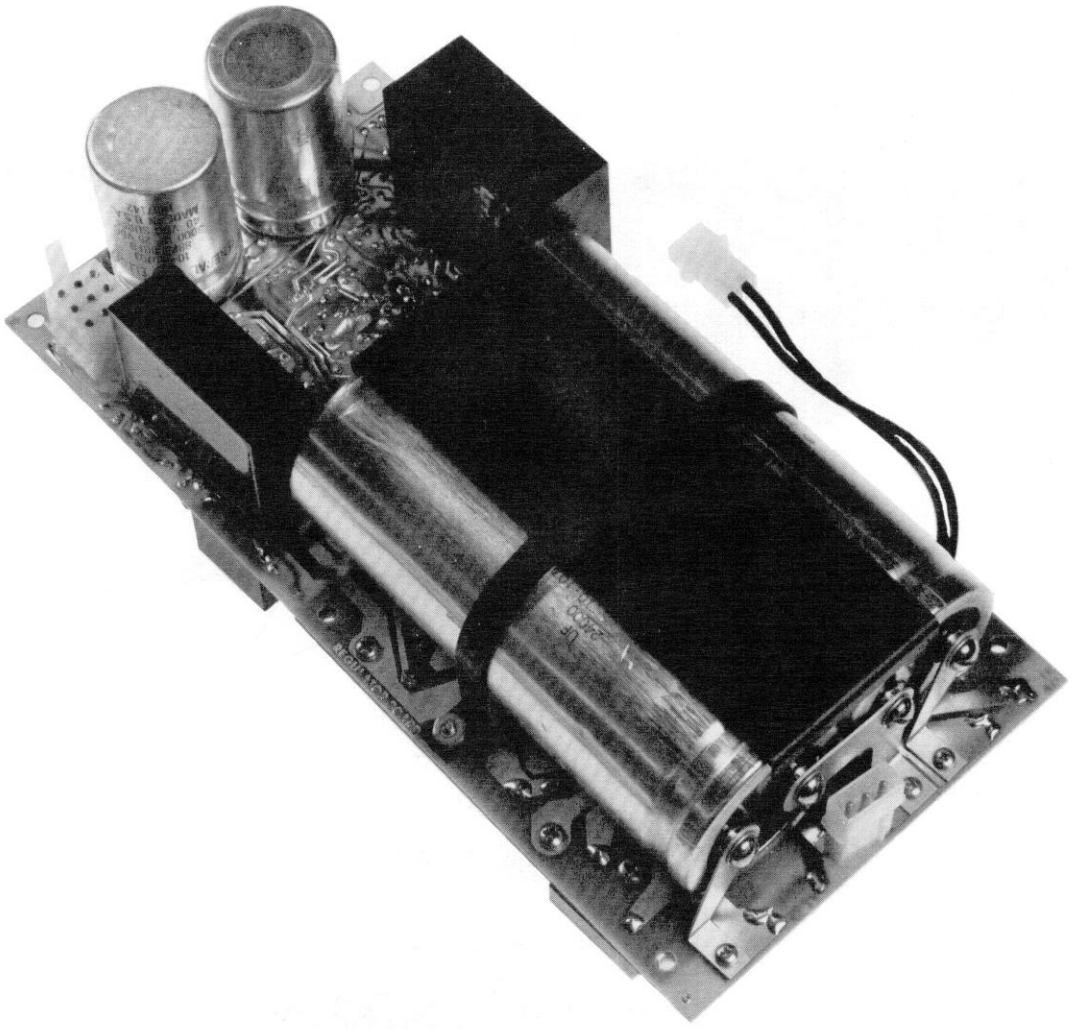
14.2.2 Power Chassis Assembly

The 700 8731 Power Chassis Assembly (Figures 14-1 and 14-2) consists of a long, inverted U-shaped chassis, 700-8726 power transformer, and a 5-inch fan. It is secured to the bottom of the computer by four 8-32 by 3/8 inch Phillips pan-head bolts.



6211-2

Figure 14-1 Power Chassis Assembly (with DC Regulator Module)



6211-1

Figure 14-2 Power Supply Assembly (with DC Regulator Module Removed)

The chassis is mounted to the right of the connector blocks, when viewed from the front, and airflow is from front to rear. The fan is held to one end of the chassis by two screws; the transformer is held to the other end by four mounting studs. The transformer may be removed by loosening four nuts, which are accessible through large holes on the bottom of the power chassis.

The dc regulator module is mounted to the chassis assembly by six screws and must be removed for cable access. The dc cable enters a slot on the connector block side of the chassis; the ac cable enters a slot on the other side.

Connections to the fan are made by small fast-tabs; connections to the transformer are made via Mate-N-Lok connectors: 6-pin for primary, 3-socket for secondary.

14.2.3 DC Regulator Module

The 5409728 DC Regulator Module (Figures 14-3 and 14-4) is a printed circuit assembly, mounted to the power chassis assembly by four 6-32 by 9/16 inch and two 6-32 by 1/4 inch Phillips pan-head screws.

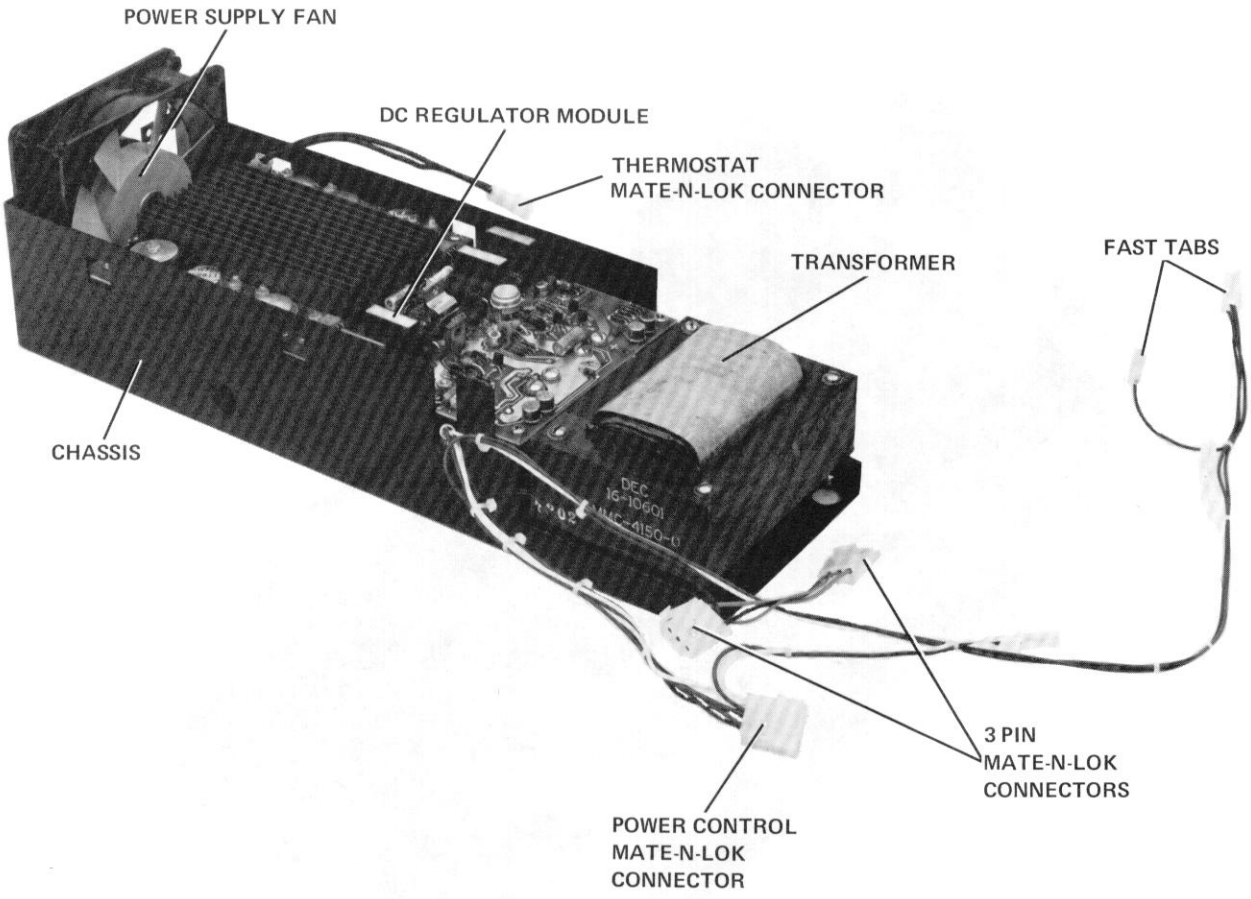


Figure 14-3 DC Regulator Module (Top View)

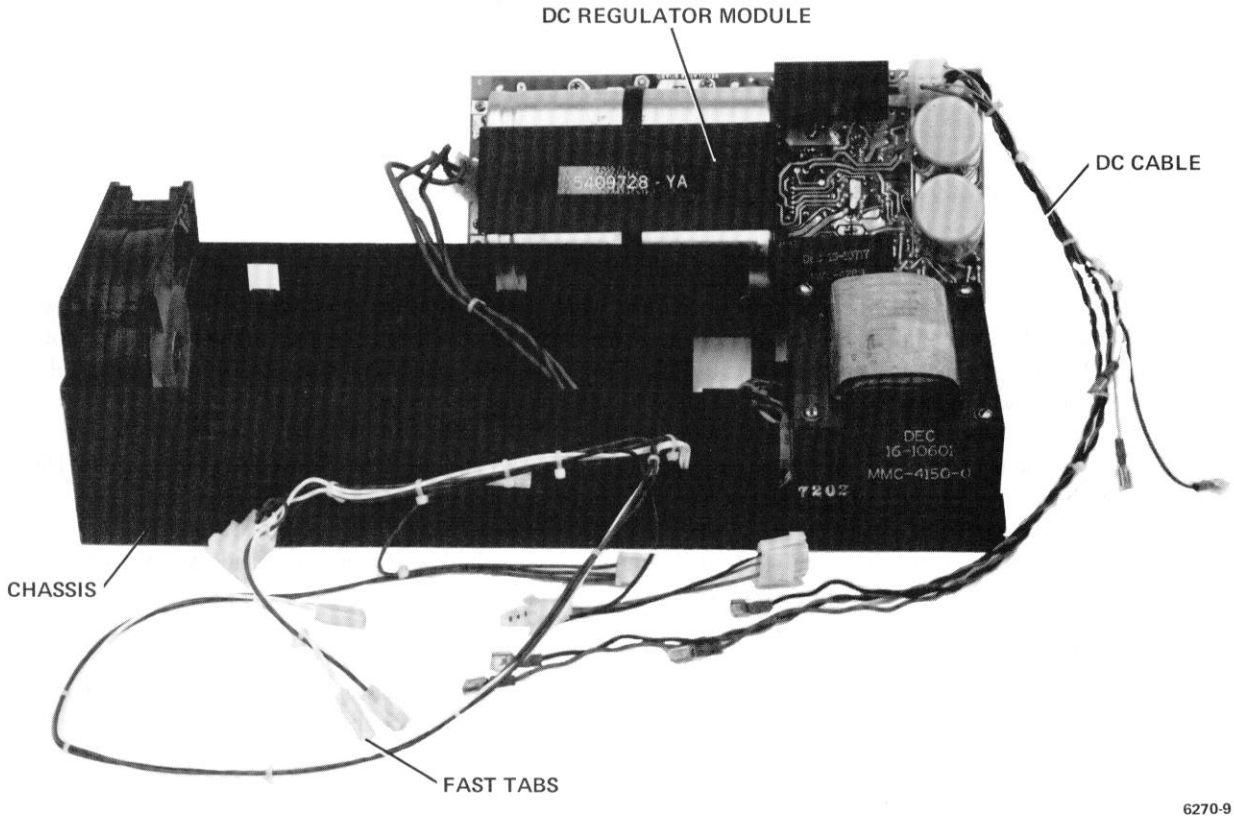


Figure 14-4 DC Regulator Module (Bottom View In Mounting Box)

Computers that were shipped during the first three or four months of production use a dc regulator module designated 5409728-YA-0; later shipments use a module designated 5409728-0-0, E revision. There are differences in component values on the two modules. The discussion of the dc regulator module circuits in this manual is directed to the later module, designated 5409728-0-0. Engineering drawings applicable to the module used are shipped with the equipment. These drawings provide schematics and component values of the dc regulator module.

This module contains all the circuitry between the transformer secondary winding and the power supply output cable. The transformer secondary 3-socket Mate-N-Lok connector is plugged into a mating connector that is soldered directly to the printed circuit board and is accessible underneath it. The 9-pin Mate-N-Lok connector on the dc output cable to the computer is similarly mated to a connector underneath the other end of the board.

The dc regulator module may be probed for troubleshooting purposes from the top; all points on the circuit are available. It may also be removed from the top for cable access and for parts replacement by removing the six mounting screws.

The printed circuit is approximately 5 by 10 inches, with about half of the top surface devoted to the heat sink. The power transistors and power rectifiers are bolted to two shelves on the sides of the heat sink and make contact with the circuit board directly underneath via solder and screw connections. The heat sink is hard anodized for electrical insulation.

The other half of the top surface is devoted to interconnecting and mounting the balance of the circuit. Three small output voltage adjustment potentiometers are accessible on this top portion of the board.

Two small pico fuses are mounted on the top of the PC board on the fan end. These fast-acting fuses will typically only blow when some component is defective or when the +5V or -15V is too high. The two input filter capacitors are held to the underside of the board by a bracket and are connected to the circuit via jumper tabs on the fan end.

The +5V and -15V output filter capacitors and inductors are also mounted under the board, the former by screws and the latter by nuts.

Care must be taken to ensure that all electrical and mechanical connections are secure. In manufacturing, the hardware is tightened with a torquing device set to 12 inch-pounds.

14.2.4 DC Cable

This is a simple cable connecting the computer module to the dc power module via a 9-pin Mate-N-Lok. The latter is made accessible by loosening the six mounting screws and lifting out the dc module. Cable access is through a slot on the computer module side of the power chassis.

14.2.5 AC Cable

This cable interconnects all ac portions of the computer chassis (Figures 14-1 through 14-4). The ac portions of the computer chassis are as follows:

a. Power Supply Fan – two fast-tabs
b. Power Supply Thermostat – one 2-pin Mate-N-Lok
c. Memory Section Fan – two fast-tabs
d. Transformer Primary – one 6-socket Mate-N-Lok
e. Power Control – one 6-pin Mate-N-Lok
f. PDP-11 System AC Power Control – two 3-pin Mate-N-Lok connectors on rear of computer.

The ac cable is located on the right-hand side and rear of the computer and is inherently shielded by the power supply chassis and the computer chassis.

14.3 SPECIFICATIONS

Tables 14-1, 14-2, and 14-3 list all the power supply specifications according to input, output, and mechanical and environmental specifications.

Table 14-1
Power Supply Input Specifications

Parameters	Specifications
*Input Voltage (1 phase, 2 wires and ground)	95–135/190–270V
Input Frequency	47–63 Hz
Input Current	5/2.5A RMS
Input Power	325W at full load
Inrush	80/40A peak, 1 cycle
Rise Time of Output Voltages	30 ms max. at full load, low line
Input Overvoltage Transient	180/360V, 1 sec 360/720V, 1 ms
Storage After Line Failure	25 ms min., starting at low line, full load
Input Breaker (part of BC05 Power Control)	7A/4A single-pole, manually reset, thermal
Thermostat Mounted on Heat Sink (opens transformer and fan power)	277V 7.2A contacts Opens 98–105°C Automatically resets 56–69°C
Input Connections	Line cord on BC05 Power Control, length and plug type specified with BC05 (Paragraph 2.2.1.1)
Turn-On/Turn-Off	Application or removal of power
Hipot (input to chassis and output)	2.1 kV/dc, 60 sec

*Input voltage selection, 115V or 230V, is made by specifying the appropriate AC Input Box, DEC Model BC05. All specifications are with respect to the BC05 input.

Table 14-2
Power Supply Output Specifications

Parameter	Specification
+15V	
Load Range	
Static	0–1A
Dynamic	0–1A
Max. Bypass Capacitance in load for 30 ms turn-on	500 mF
Overvoltage protection	None
Current limit at 25°C	1.3A to 1.7A (−6.2 mA/°C)
Backup Fuse	15A (also used for +5V)
Adjustment	±5% min.
Regulation (All causes including line, load, ripple, noise, drift, ambient temperature)	±5%
+5V	
Load Range	
Static	0–15A
Dynamic #1	±5A (within 0–17A load range)
Dynamic #2	No load – full load
Max. Bypass Capacitance in load for 30-ms turn-on	2000 μF
Overvoltage Crowbar (blows fuse)	5.7–6.8V actuate (7V abs. max. output)
Current Limit at 25°C	24–29.4A (−0.1A/°C)
Backup Fuse (series with raw dc)	15A
Adjustment Range	±5% min.
Regulation	
Line	±0.5%
Static Load	3%
Dynamic Load #1	±2%
Dynamic Load #2	±10%
Ripple and Noise	4% peak-to-peak
1000 Hour Drift	±0.25%
Temperature (0–60°)	±1%

Table 14-2 (Cont)
Power Supply Output Specifications

Parameter	Specification
-15V	
Load Range	
Static	0–7A
Dynamic #1	ΔI = 5A (0.5A/μs)
Dynamic #2	No load – full load (0.5A/μs)
Max. Bypass Capacitance in load for 30-ms turn-on	1000 μF
Overvoltage Crowbar (blows fuse)	17.4–20.5V (22V abs. max. output)
Current Limit at 25°C	10–13.3A (-0.03A/°C)
Backup Fuse (series with raw dc)	5A
Adjustment Range	±5% min.
Regulation	
Line and Static Load	±1%
Dynamic Load #1	±2.5%
Dynamic Load #2	±3%
Ripple and Noise	3% peak-to-peak
1000 Hour Drift	±0.25%
Temperature (0–60°C)	±1%
BUS DC LO L and BUS AC LO L	
Static Performance at Full Load (for 230V connection, double below voltages)	
BUS DC LO L goes to high	74–80 Vac line voltage
BUS AC LO L goes to high	8–11V higher
BUS AC LO L drops to low	80–86 Vac line voltage
BUS DC LO L drops to low	7–10V lower
Hysteresis (contained in above specifications)	3–4 Vac
Output voltages still good	70 Vac line voltage

Table 14-2 (Cont)
Power Supply Output Specifications

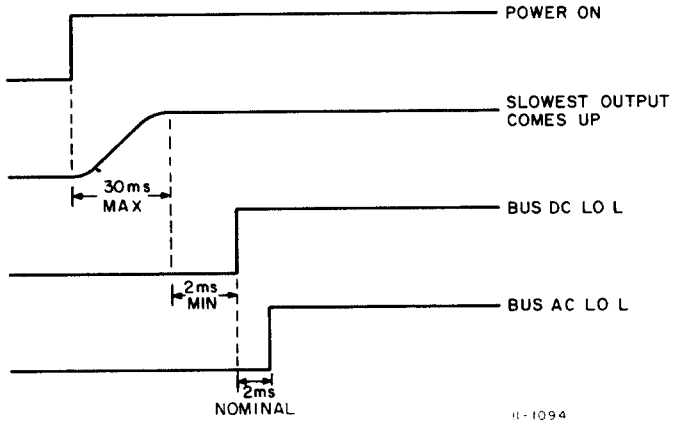
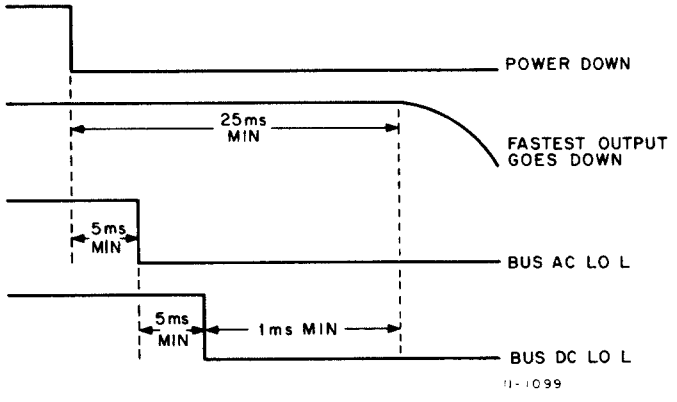
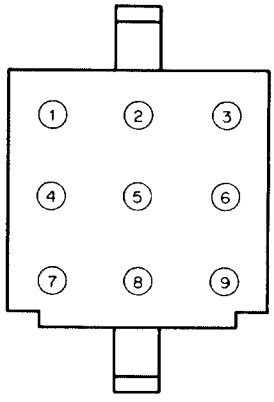
Parameter	Specification
BUS DC LO L and BUS AC LO L (Cont)	
Dynamic Performance	
Worst case on power-up is high line, full load.	
Worst case on power-down is low line, full load.	
Output Characteristics	
Open Collector	50 mA sinking capability +0.4V max. offset
Pull-Up Voltage on Unibus	5V nominal, 180Ω impedance
Rise and Fall Times	1 μs max. Outputs shall remain in 0 state subsequent to power failure until power is restored despite Unibus pulling voltages remaining.

Table 14-3
Mechanical and Environmental Specifications

Parameter	Specification
Weight	
DC Regulator	7 lb approx.
Power Chassis Assembly including AC Regulator Module	18 lb approx.
Dimensions	16.50 in. length 5.19 in. width 3.25 in. height
Cooling Means	Integral 5 in. fan
Minimum Cooling Requirements	375 CFM through heat sink 250 CFM over caps, chokes, and transformer
Rated Heat Sink Temperature	95°C max.
Shock, Non-Operating	40G (duration 30 ms) 1/2 sine in each of six orientations
Vibration, Non-Operating	1.89G RMS average, 8G peak; varying from 10 to 50 Hz, 8 dB/octave roll-off 50–200 Hz; each of six directions
Ambient Temperature	0 to +60°C operating -40 to +71°C storage
Relative Humidity	95% max. (without condensation)
Altitude	10K ft

Output parameters are specified at the pins of the 9-pin Mate-N-Lok connector (Figure 14-5) which plugs into the output connector on the 5409728 module. All output voltages are given with respect to the common ground pin on this connector. IR drops in the distribution wiring are minimized to achieve good regulation at the load.

Pin 1 BUS AC LO L
Pin 2 Common
Pin 3 +5V output
Pin 4 LTCL (Clock Signal)
Pin 5 +15V output
Pin 6 BUS DC LO L
Pin 7 Not used
Pin 8 Not used
Pin 9 -15V output



NOTES:
1. The circuit connected to pins 7 and 8 is not used in the PDP-11.
2. Pin 2 is not connected to chassis within the power supply. Chassis ground is made at the backplane.

Figure 14-5 Output Connector, 5409728 Regulator Module

CHAPTER 15
POWER SUPPLY DETAILED DESCRIPTION

15.1 INTRODUCTION

The power supply is divided into two sections: the ac input circuit and the dc regulator module. A detailed description to the circuit level is provided for each section. The ac input circuit description discusses the power supply interconnections, power control, power switch, transformer, power control circuit breaker, and the power supply thermostat. The dc regulator module operation description discusses the generation at the circuit level of each of the five power supply outputs.

15.2 AC INPUT CIRCUIT

A detailed ac interconnection diagram is shown in Figure 15-1. Figures 15-2 and 15-3 give this information in schematic form.

The line cord, single pole breaker, RFI capacitors, and connections for transformer 115V or 230V wiring are contained in the power control unit. To select 115V input or 230V input, use the BC05H or BC05J power control unit, respectively.

A 3-section managed keyswitch is employed and mounted on the console. One section interrupts the power to the transformer primary. A second section is wired to two 3-pin Mate-N-Loks; if the PDP-11 cabinet power control bus is plugged into one of these connectors, the keyswitch will turn on the whole cabinet as well as the computer. The other three-pin Mate-N-Lok is provided for daisy-chaining in the cabinet power control system. The third section of the keyswitch is for Panel Lock and is described in Chapter 4.

The transformer is rated for 47-63 Hz and is equipped with two windings that are connected by the power control in parallel for 115V operation and in series for 230V. The fans are connected across half of the primary so that they are always provided with 115V nominal. There is an electrostatic shield between primary and secondary of the transformer.

The power control circuit breaker contains a single-pole thermal circuit breaker that protects against input overload and is reset by pressing a button on the rear of the computer.

The thermostat is mounted on the power supply heat sink. If the heat sink temperature rises to about 100°C, the thermostat will open one side of the primary circuit and de-energize the power supply. It will automatically reset at about 64°C.

15.3 DC REGULATOR MODULE OPERATION

The discussion of the DC Regulator Module circuits in this manual is directed to the module designated 5409728-0-0, rather than the earlier module designated 5409728-YA-0. A block diagram of this module is shown in Figure 15-4. The center tapped output of the power transformer is applied to positive and negative rectifier and filter circuits. The rectifier circuits produce +28V and -28V nominal raw dc voltages which are unregulated but well filtered by the input storage capacitors.

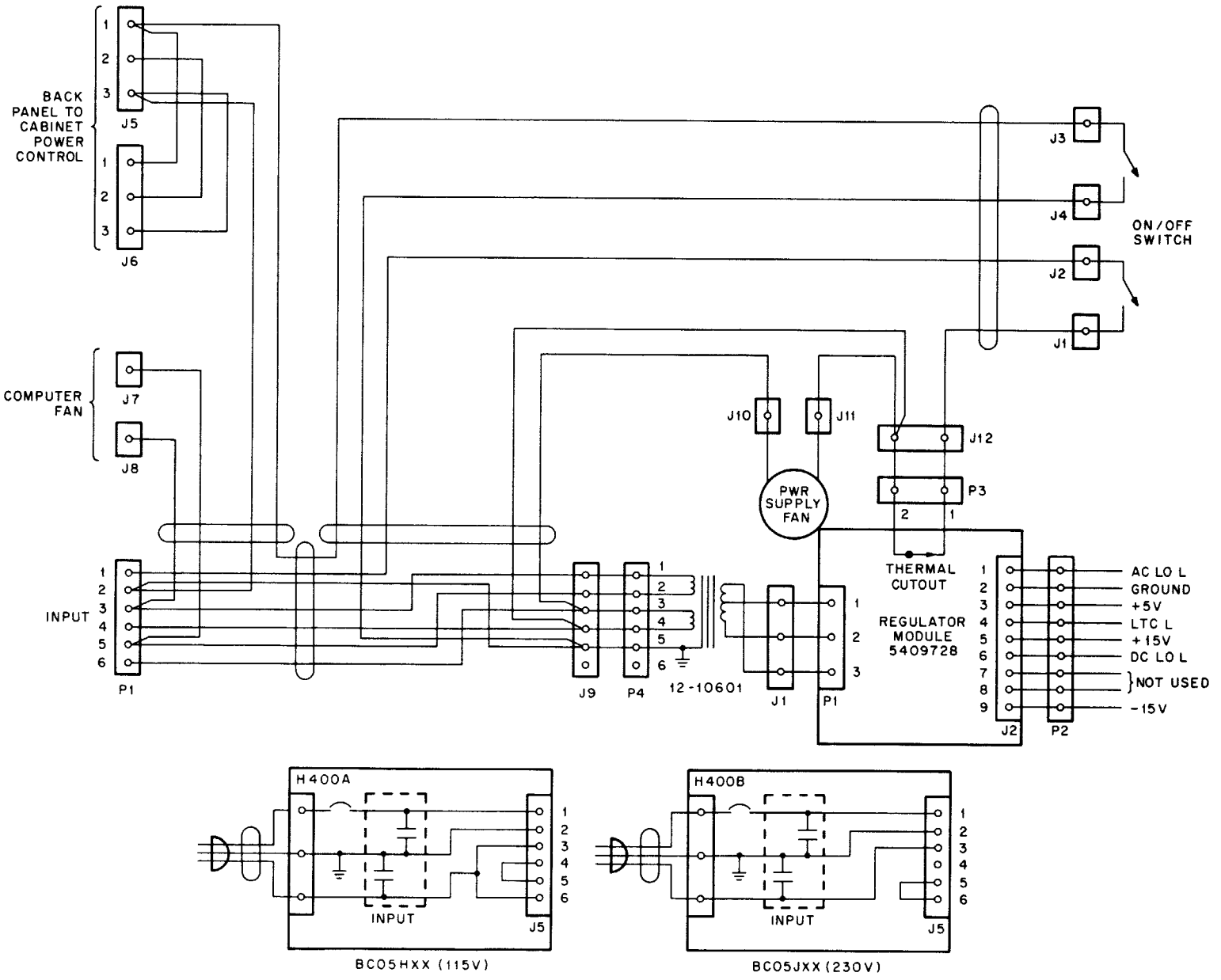


Figure 15-1 Detailed AC Interconnection Diagram

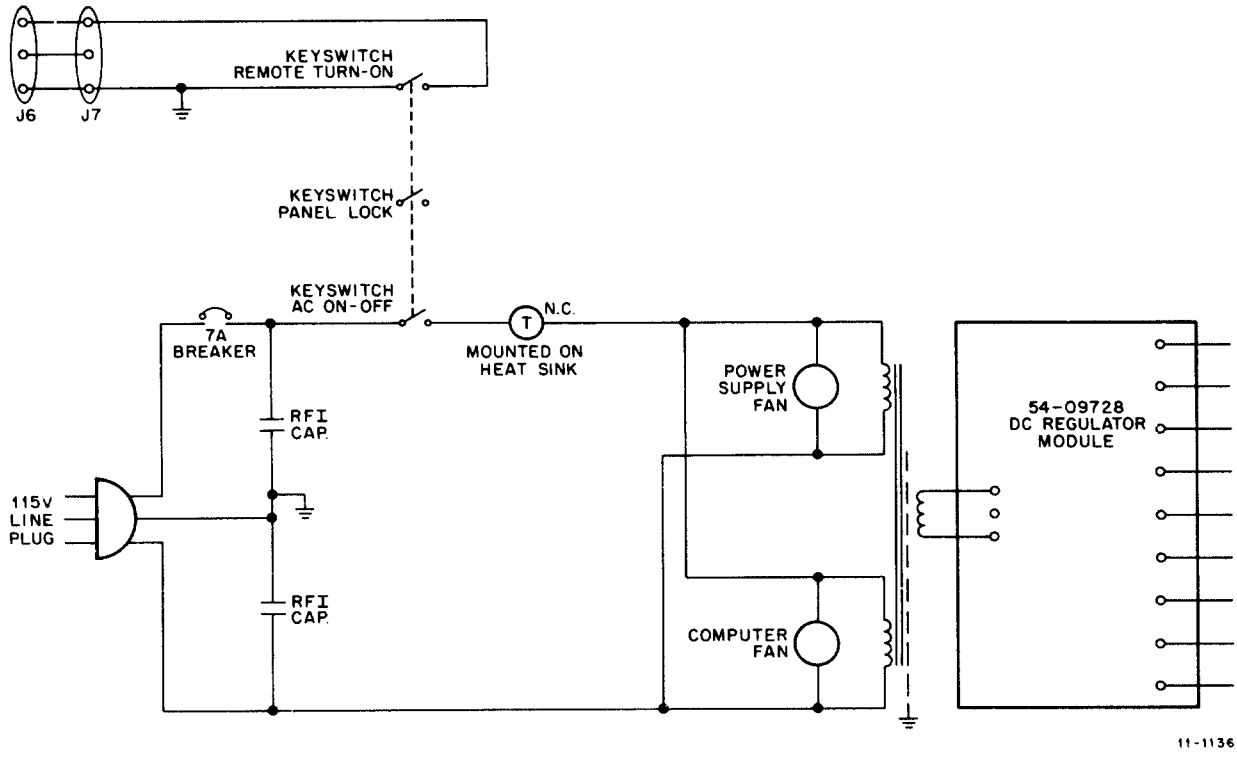


Figure 15-2 115V Connections – Simplified Schematic Diagram

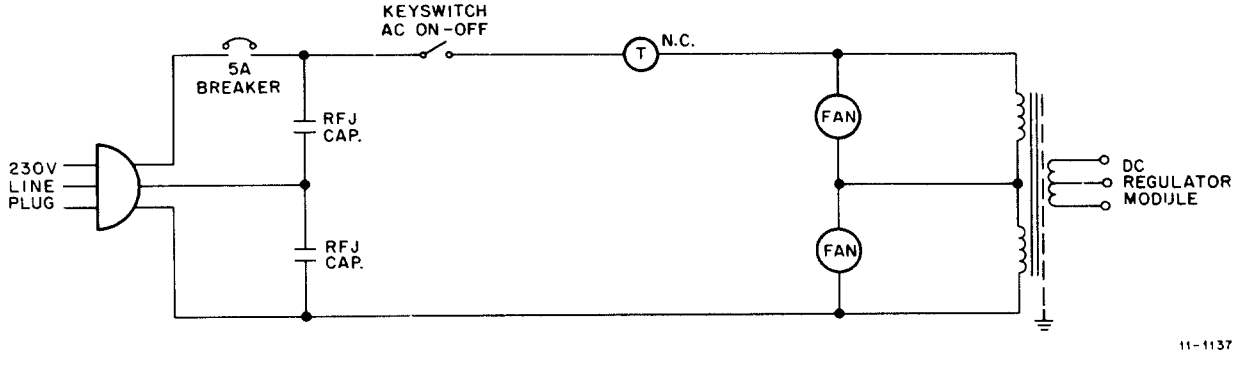


Figure 15-3 230V Connection Diagram

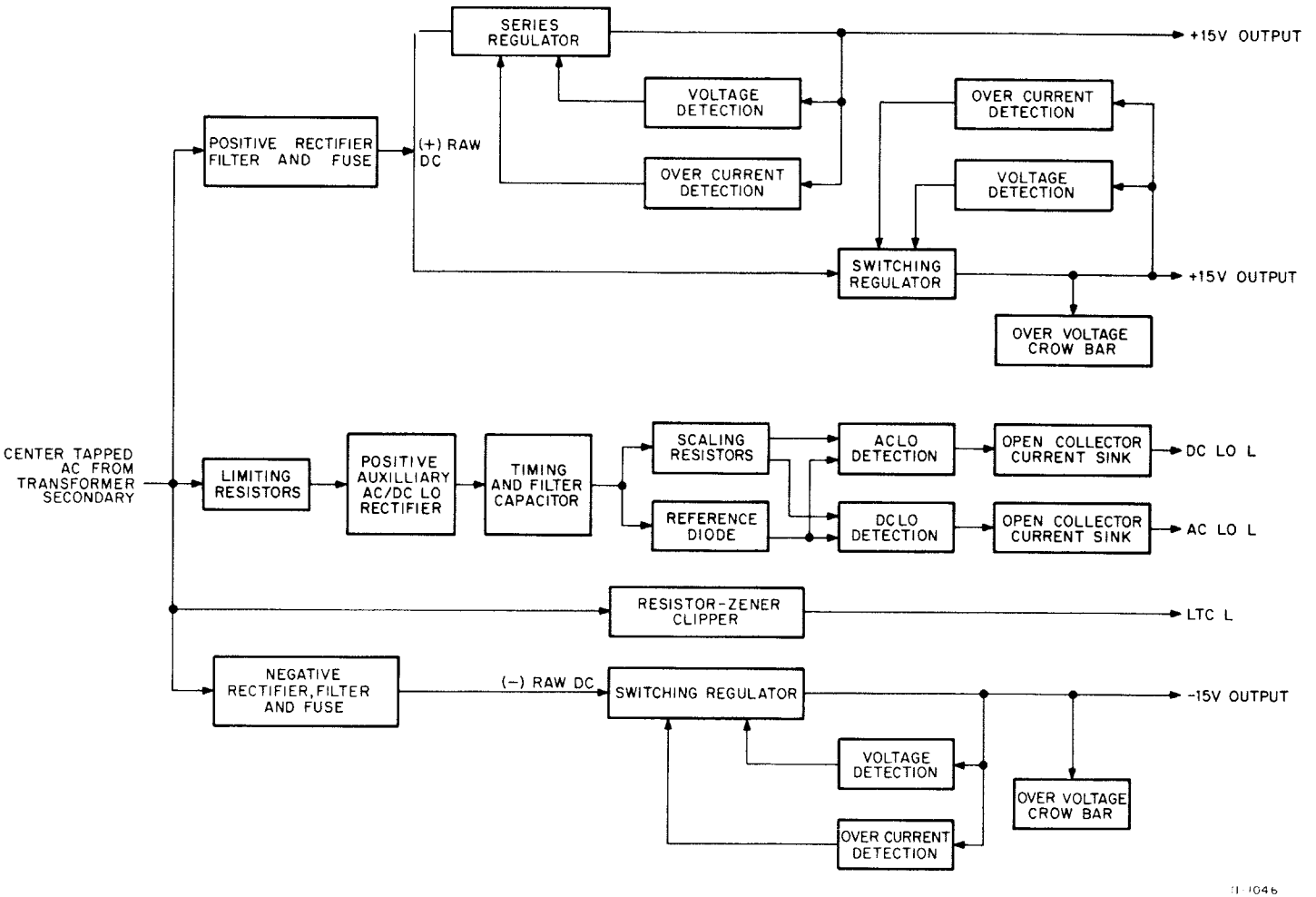


Figure 15-4 Regulator Module Block Diagram

The +28V dc is used by an efficient switching regulator circuit to produce the +5V dc output. Provisions for overcurrent detection are incorporated in the regulator circuit so that excess current is limited when there is a malfunction in the load. The +5V output is also protected against overvoltage by a crowbar circuit which limits the output to under 7V; before the output gets to this value the crowbar circuit blows the fuse in the output circuit of the rectifier.

The -28V dc is used by the -15V circuit, which is similar in operation to the +5V regulator circuit. The -15V crowbar circuit limits the output to 22V.

The LTC L Real-Time Clock synchronizing signal is generated by a simple Zener clipper that is fed from the transformer secondary.

The BUS AC LO L and BUS DC LO L signals are used to warn the Unibus of imminent power failure. Circuits on the regulator module detect the transformer secondary voltage and generate two timed TTL-compatible open-collector signals that are used for power fail functions by devices on the Unibus.

15.3.1 Generation of ±Raw DC

As stated in the previous paragraph, the centertapped transformer secondary voltage is rectified and filtered prior to being fed to the three dc regulators.

The circuitry involved is shown in Figure 15-5. The bridge rectifier D14 is mounted on the heat sink and the input capacitors C1 and C2 are mounted on the bottom of the regulator module. These capacitors filter the input dc and are large enough to provide at least 25-ms storage when the input power is shut off or fails.

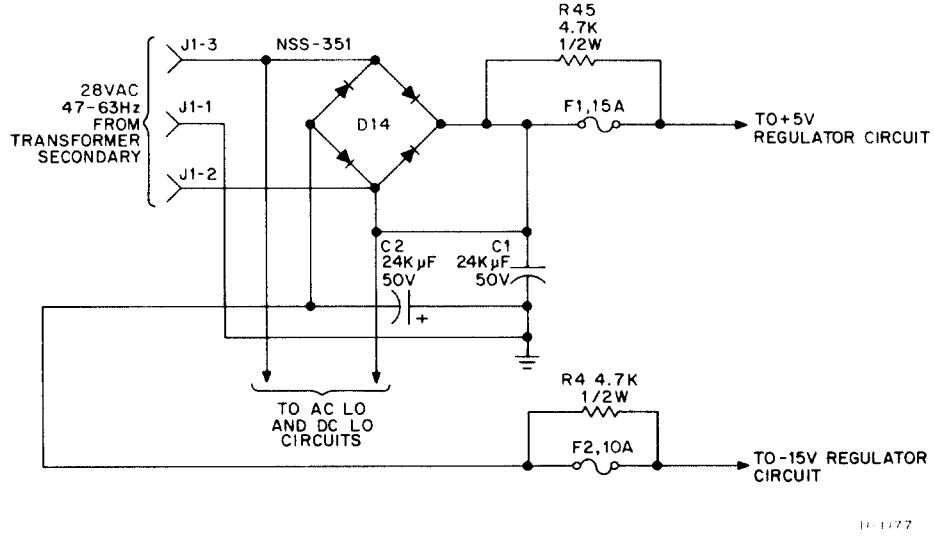


Figure 15-5 Rectifier and LTC L Circuits

A fuse is used on each output to protect the regulator and load during faults. The fuses will not normally blow when a regulator output is shorted because the three outputs are electronically overcurrent protected. However, the appropriate fuse will blow in case of +5V or -15V overvoltage crowbar or in case of failure in one of the overcurrent circuits.

The resistor across each fuse provides a slow (100 - 150 seconds) discharge of C1 or C2 after the power is turned off in case a fuse blows. The capacitors are placed ahead of the fuse to limit the energy in any fault and thus better protect the outputs.

15.3.2 LTC L Circuit

The LTC L Real-Time Clock synchronizing signal (Figure 15-3) is generated by a Zener clipper circuit. The output waveform is a square (clipped sine) wave at line frequency. For one polarity of output sine wave, D13 clips at about +3.9V and in the other polarity D13 clips at its forward voltage of -0.7V.

15.3.3 BUS AC LO L and BUS DC LO L Circuits

The circuitry shown in Figure 15-6 is employed to generate the timed Unibus power status signals specified in Tabie 14-2. These are used for power fail functions. The transformer secondary voltage is rectified by D1 and D2 and filtered by C9 and R1, R14.

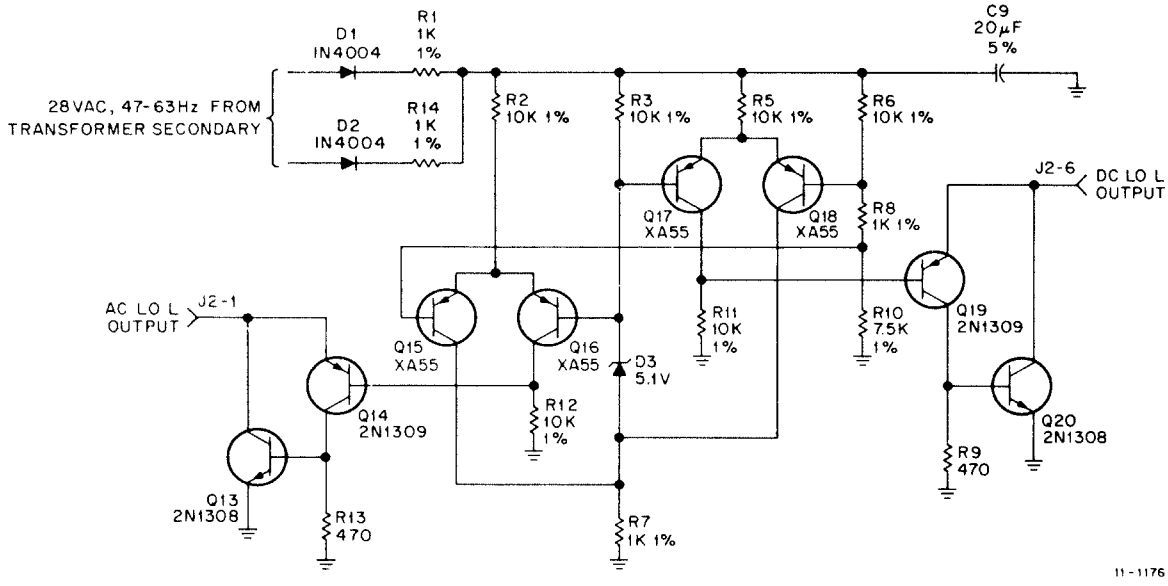


Figure 15-6 BUS AC LO and BUS DC LO Circuits

Circuit parameters are chosen so that the voltage across C9 will rise slower than the three regulated output voltages on power-up, and will decay faster than the three regulated output voltages on power-down.

Two differential amplifier circuits are used to detect power status: C17, Q18 is used to generate BUS DC LO L; and Q15, Q16 is used to generate BUS AC LO L. The differential amplifiers share a common reference Zener diode D3, which is fed approximately 1 mA by R3.

As C9 charges subsequent to power-up, first Q17, Q18, and then Q15, Q16 change state; the reverse is true during power-down. When C9 starts to charge, Q17 and Q16 are on and Q15 and Q18 are not conducting. As C9 charges further, Q18 starts to conduct into R7 and raises the voltage on cathode D3. This acts as positive feedback and snaps Q17 off and Q18 on more solidly. A few milliseconds later, the voltage across C9 has risen sufficiently for the same process to take place in differential amplifier Q15, Q16. The status of each differential amplifier is followed by the germanium transistor open-collector output stages Q19, Q20 for BUS DC LO L, and Q13, Q14 for BUS AC LO L. These stages clamp the Unibus at about +0.4V until the differential amplifier circuits sequentially signal them across R11 and R12 that power is up. The outputs then rise to about +5V as dictated by the Unibus loading and pull-up termination resistors.

The sequence is as follows:

power-up → then BUS DC LO L = 0 → then BUS AC LO L = 0
0 = High (+3V)

power-down → BUS AC LO L = 1 → BUS DC LO L = 1
1 = low (+0.4V)

Any time that BUS DC LO L or BUS AC LO L go low, there is sufficient storage in capacitors C1 and C2 to maintain output voltage long enough to permit the power fail circuit to operate. The open collector stages are designed to clamp the Unibus to 0.4V maximum, even when there is no ac input to the regulator. They are inherently biased on by R11 and R12 until the differential amplifiers signal that power is OK.

15.3.4 +15V Regulator Circuit

The +15V regulator shown in Figure 15-7 is a simple series regulator. The pass transistor Q1 is a high-gain power Darlington and is mounted on the heat sink. Base drive current is supplied to Q1 via R38. Q3 acts to limit the value of this current to the required value by shunting it away from the Q1 base. Q4, the voltage detector amplifier, biases on Q3 and thus limits current in Q1. The +15V output voltage is sampled on the viewing chain R34, 35, 36 and compared to the voltage across reference Zener D8, which is fed by R37. If the output should try to increase from the regulated value, the emitter of Q4 is made more negative (relatively) than its base and conduction through Q4 increases. This increases the conduction through Q3 and causes Q1 to shut down sufficiently to restore the output voltage to the regulated value. Ambient temperature compensation of the voltage detector is essentially flat since D8 has a +2 mV/°C temperature coefficient and the base emitter junction of Q4 has a -2 mV/°C temperature coefficient.

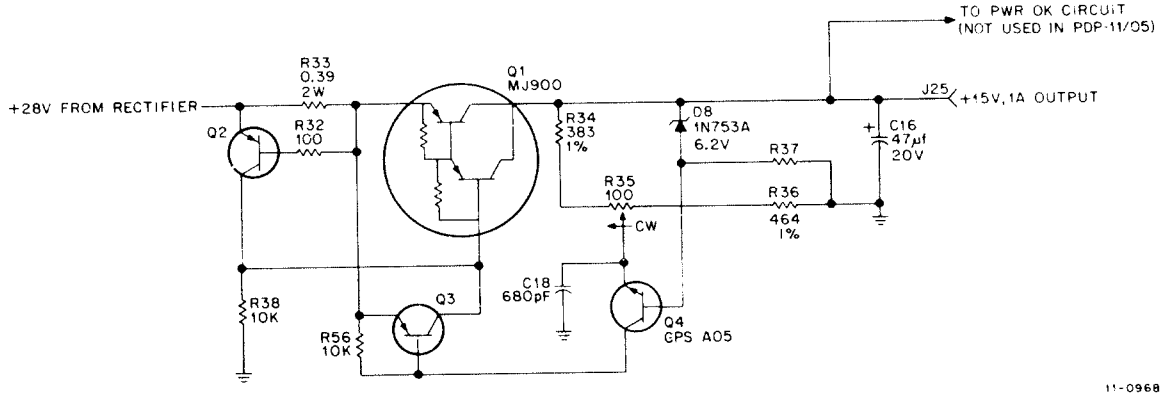


Figure 15-7 +15V Regulator Circuit

R35 acts as the +15V voltage adjustment potentiometer. C18 is a high frequency stabilization capacitor. Q2 is the overload detector; when the output current reaches 1.5A nominal, the voltage across R33 is sufficient to cause Q2 to conduct. This removes base drive from Q1 and causes the regulator to current limit.

15.3.5 +5V Regulator Circuit

The +5V regulator is similar to the +15V regulator in that the sampled output voltage is compared to the voltage across a reference Zener by a voltage detector transistor, which in turn controls the drivers for the main pass transistor. The +5V regulator circuit is shown in Figure 15-8. An over-current circuit is likewise employed.

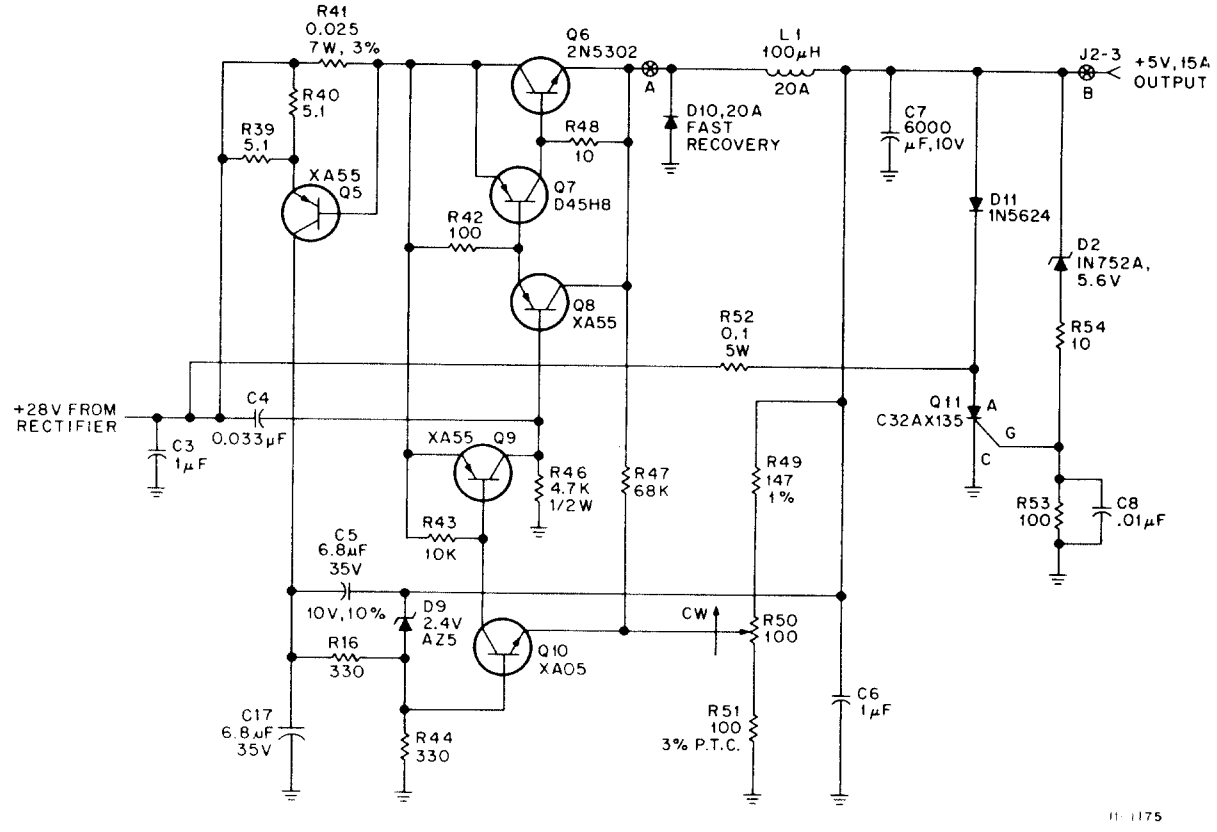


Figure 15-8 +5V Regulator Circuit

The viewing chain consists of R49, 50, 51 and the reference Zener is D9, which is fed by R44. Q10 is the detector amplifier. The pass transistor Q6 and first stage driver Q7 are mounted on the heat sink. The predriver Q8 is turned on by R46. The current is diverted from the base of Q8 by off-driver Q9, which is controlled by Q10. The +15V and +5V regulators are similar in operation; i.e., a tendency for the output voltage to rise results in more conduction through Q10 and resultant limiting of conduction through Q6.

Here the similarity ends. The +5V circuit is a regulator that operates in the switching mode for increased efficiency. To get the regulator to switch, positive feedback is applied to the voltage detector input via R47. Thus the whole regulator acts as a power Schmitt trigger and is either completely turned on or turned off, depending on whether the output voltage is too high or too low. When Q6 is on, it supplies current through filter choke L1 to the output smoothing capacitor C7 and the load. When Q6 is off, the L1 current decays through commutating diode D10, which becomes forward biased by the back emf of L1. The waveform across D10 is a 30V nominal rectangular pulse train. The filtered output across C7 is thus +5 Vdc with about a 200-mV peak-to-peak 10-kHz nominal sawtooth of super-imposed ripple. At the crest of the ripple, Q6 turns off and at the valley Q6 turns on. This switching mode of operation limits the dissipation in the circuit to the saturated forward losses of Q6 and D10 and the switching losses of Q6. The resultant high efficiency allows the heat sink to be small and the number 8 power semiconductors to be few.

R50 is the voltage adjustment potentiometer. R51 is a positive temperature coefficient wire-wound resistor that compensates for the fact that the Q10 base-emitter junction and the reference diode D9 both have negative voltage temperature coefficients. Q5 current, limited by R39, 40, detects the overcurrent signal generated across resistor R41, which is in series with the Q6 collector.

Output fault current is limited to a safe value because conduction of Q5 makes the reference voltage across D9 decrease to zero. This causes Q10 to conduct and shuts down the regulator. C5 is an averaging capacitor, which is necessary in the circuit because the current through R41 is pulsating.

High frequency bypass capacitors are used on input and output of the regulator, C3 and C6, respectively. C4 is used to slow down the turn-on of Q6 to allow D10 to recover from the on state without a large reverse current spike.

In the event a malfunction causes the output voltage to increase beyond about 6.8V nominal, Zener diode D2 will conduct and fire silicon-controlled rectifier Q11. This will crowbar the output voltage to a low value through D11 and will blow fuse F1 in the rectifier circuit through R52.

15.3.6 -15V Regulator Circuit

The -15V regulator circuit is shown in Figure 15-9. It is essentially the complement of the +5V regulator circuit and differs only in minor detail.

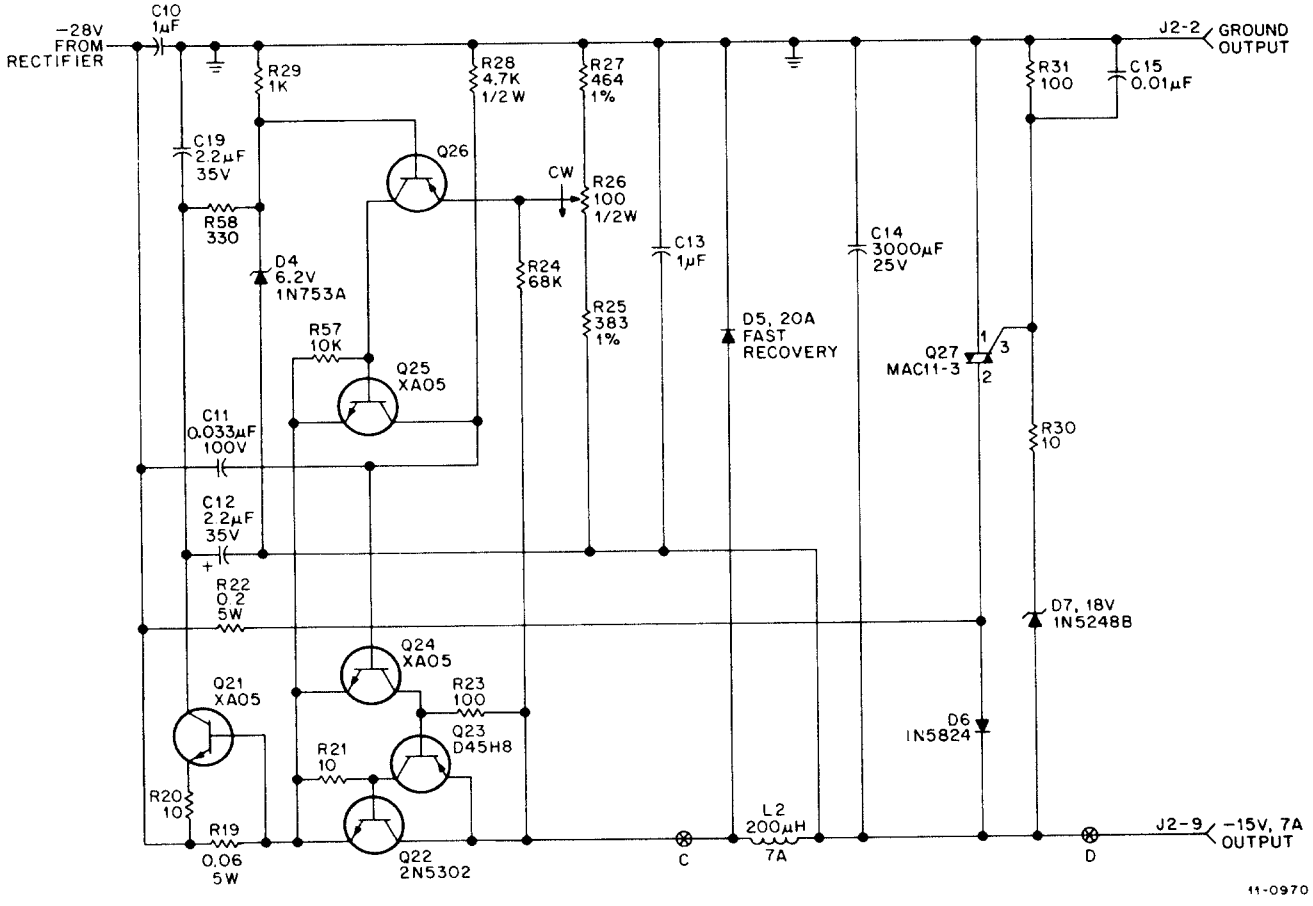


Figure 15-9 -15V Regulator Circuit

The crowbar device is a Triac Q27 instead of an SCR. No temperature compensating resistor is required because Q26 and D4 track each other, as in the +15V regulator (Paragraph 15.3.4). The detailed interconnection of the drivers and the circuit values are different. The -15V output voltage is adjusted by potentiometer R26.

CHAPTER 16
POWER SUPPLY MAINTENANCE

16.1 INTRODUCTION

Information is provided in this chapter to maintain the power supply. This consists of adjustments, circuit waveforms, troubleshooting, and parts identification. The adjustments consist of three output potentiometers. The circuit waveforms provide a guide to proper operation at various places in the circuit. The troubleshooting section provides rules, hints, and a troubleshooting chart as a maintenance aid in isolating power supply malfunctions. Finally, the parts identification section provides a directive to obtaining parts information for the entire power supply unit through a parts location directory to the mechanical engineering drawings in the *Engineering Drawing Manual.*

16.2 ADJUSTMENTS

Three adjustments to the power supply adjust the three dc output voltages: +15V, +5V, and -15V. A small screwdriver is all that is required. Clockwise adjustment of any of the potentiometers increases voltage, and the potentiometers are located on the top side of the dc regulator module. The potentiometer designations are:

a. R35 – +15V
b. R50 – +5V
c. R26 – -15V

In performing any of these adjustments note the following:

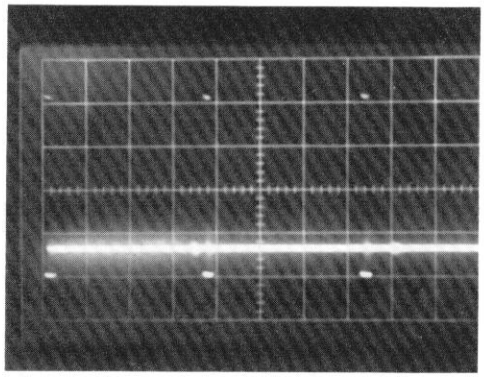
CAUTION

1. **Do not adjust voltages beyond their 105 percent rating and adjust slowly in order to avoid overvoltage crowbar, which will blow dc output fuses.**

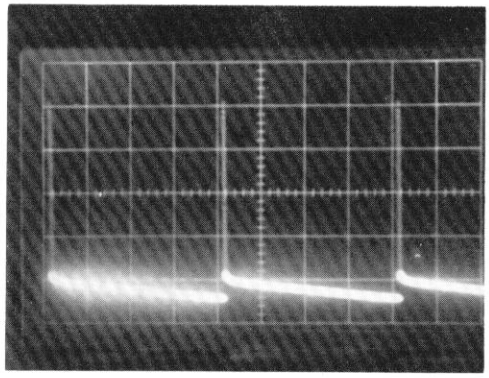
2. **Do use a calibrated voltmeter; preferably a digital voltmeter. Voltages should be adjusted to their center values: +15.0, +5.0, and -15.0, all under load at the dc cable termination on the system unit.**

16.3 CIRCUIT WAVEFORMS

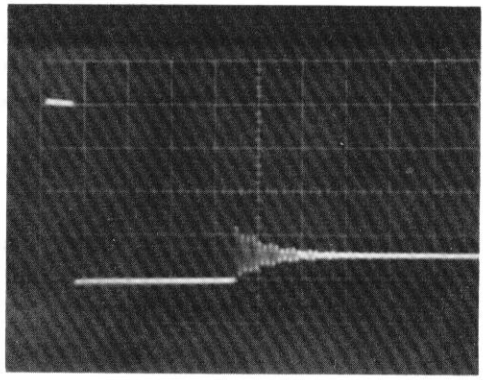
The two basic regulator circuits used on the dc regulator module generate +5V and -15V. Figure 16-1 shows six waveforms of the +5V regulator circuit taken at two points (A and B) in the circuit (Figure 14-6). Waveforms a, b, and c are taken at point A, which is the +5V circuit, Q6 transistor output. Waveforms d, e, and f are taken at point B, which is +5V power supply output (J2-3). Figure 16-1 also indicates the load conditions and time scales for each waveform. Figure 16-2 shows six waveforms of the -15V regulator circuit taken at two points (C and D) in the circuit (Figure 14-7). Waveforms a, b, and c are taken at point C, which is the -15V power supply output (J2-9). The load conditions and time scales of the respective waveforms are indicated in Figure 16-2. These waveforms were taken on a Tektronix Model 453 Oscilloscope. All waveforms are with respect to J2-2, power common.



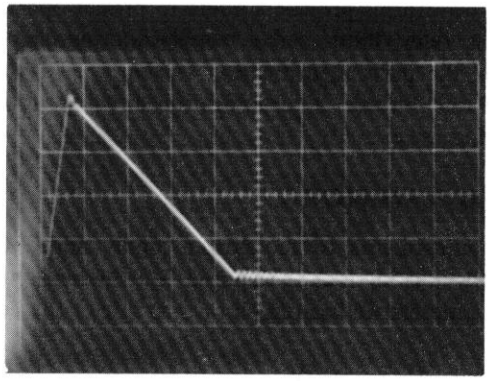
a) Point A, No load,
2 ms /div, and
10V/div.



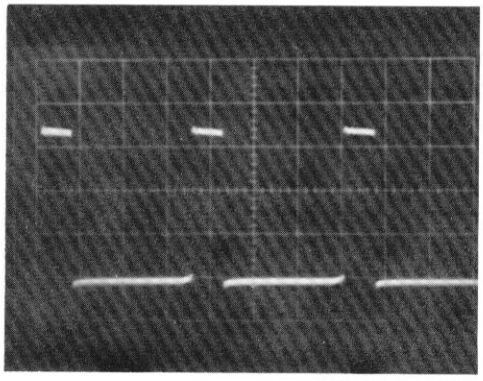
d) Point B, No load,
2 ms/div, and
50 mV/div.



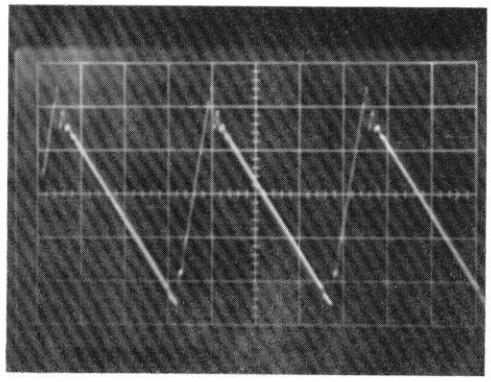
b) Point A, No load,
20 μs/div, and
10V/div.



e) Point B, No load,
20 μs/div, and
50 mV/div.

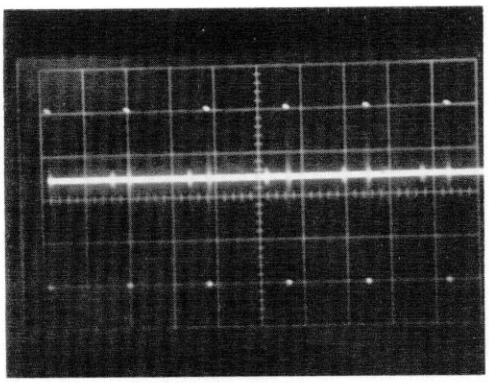


c) Point A, 20A load,
20 μs/div, and
10V/div.

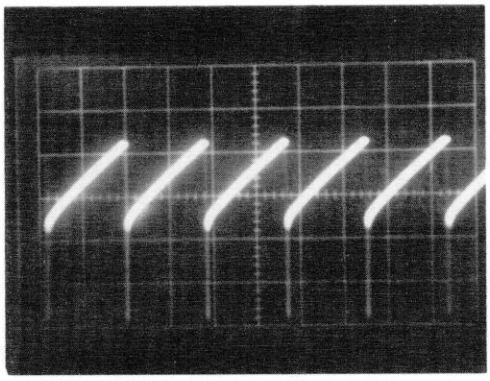


f) Point B, 20A load,
μs/div, and
50 mV/div.

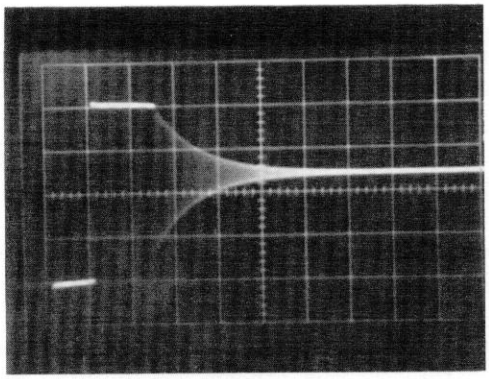
Figure 16-1 +5V Regulator Circuit Waveforms



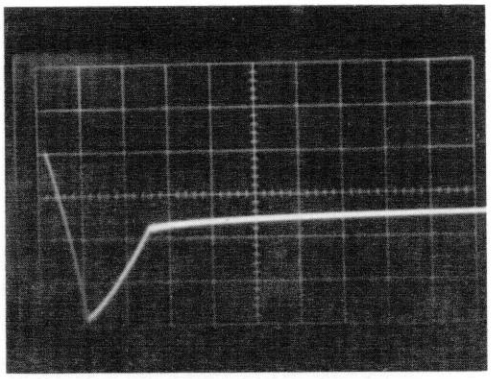
a) Point C, No load,
5 ms/div, and
10V/div.



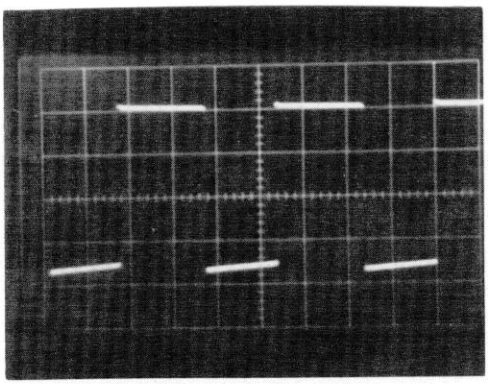
d) Point D, No load,
5 ms/div, and
50 mV/div.



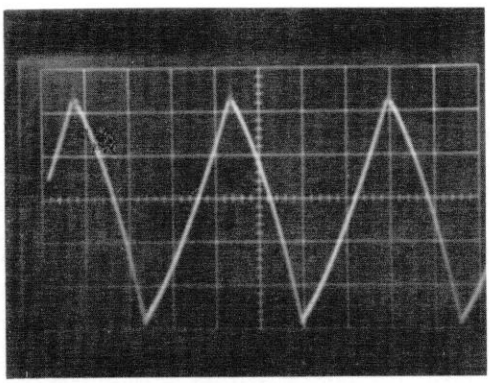
b) Point C, No load,
50 μs/div, and
10V/div.



e) Point D, No load,
50 μs/div, and
50 mV/div.



c) Point C, 5A load,
50 μs/div, and
10V/div.



f) Point D, 5A load,
50 μs/div, and
50 mV/div.

Figure 16-2 -15V Regulator Circuit Waveforms

16.4 TROUBLESHOOTING

Troubleshooting information for the power supply consists of troubleshooting rules, hints, and a troubleshooting chart. This information provides a maintenance aid to isolating power supply malfunctions (drawing D-CS-5409728-0-1).

16.4.1 Troubleshooting Rules

Troubleshooting rules for the power supply are as follows:

a. Make certain that power is turned off and unplugged before servicing the power supply.

b. Ensure that input capacitors C1 and C2 are discharged before servicing the power supply. A 10 to 100Ω, 10W resistor can be used to hasten the discharge of the capacitors. (Be sure power is off.)

c. The dc regulator module is not internally grounded to the chassis; therefore, shorts to ground can be located after disconnecting the dc output cable to the system unit.

d. The dc output fuses F1 and F2 can be replaced without removing the dc regulator module. Before unsoldering fuses, observe cautions described in Steps a and b.

e. For proper operation, all hardware must be secured tightly to about 12 inch-pounds (i.e., capacitors, chokes, semiconductors). All hardware should be replaced with identical hardware replacement parts.

f. The dc regulator module may be removed from the top of the power chassis assembly while the latter is still bolted to the computer chassis. The dc regulator module is held in place by six screws.

g. When replacing power semiconductor components that are secured to the heat sink, apply a thin coat of Wakefield #128 compound or Dow Silicon Grease to the heat sink contact side (bottom) of the semiconductor. Insulating wafers are not required.

16.4.2 Troubleshooting Hints

CAUTION
Unplug computer before servicing.

The most likely source of power supply malfunction is the dc regulator module. A quick remedy for a malfunction may be to replace this entire module. The problem, however, could be a short in the system unit or possibly a defective component or other problem in the ac input circuit.

The +5V and -15V regulators contain overvoltage detection circuitry. If R50 or R26 are adjusted too far clockwise, the corresponding crowbar circuit will trip and blow fuses. To correct this condition: adjust the potentiometer fully counterclockwise, replace the blown fuse, and re-adjust per Paragraph 16.2.

Make a visual examination of the circuitry. Check for burnt resistors, cracked transistors, burnt printed circuit board etch, oil leaking from capacitors, and loose connections. A visual check can be a quick method of locating the cause of a malfunction.

16.4.3 Troubleshooting Chart

In checking the various areas of the power supply, the rules listed in Paragraph 16.4.1 should be followed. The waveforms referenced in Paragraph 16.3 provide a comparison for the troubleshooting readings. Table 16-1 provides the dc regulator troubleshooting chart.

Table 16-1
Troubleshooting Chart

Problem	Cause
No +5V and +15V output	F1 opened* D14 or transformer opened* +5V adjusted too high*
+5V Output Too Low	Q5, D9, Q10, Q9, Q11, D12, or D10 Shorted C5 or C7 shorted R49, R50, R46, or R44 opened Q6, Q7, Q8, or D11 shorted A9, Q10, or D9 opened* R51, or R50 opened
+15V Output Too High	Q1 shorted E8 opened R35 or R36 opened
No -15V Output	F2 opened D14 or transformer opened
-15V Output Too Low	-15V adjusted too high* Q25, D4, Q26, Q21, Q27, D7 or D5 shorted C14 or C12 shorted R22, R26, R25, or R29 opened Q22, Q23, Q24, or D6 shorted Q25, Q26, or D4 opened
BUS AC LO L Will Not Go High	Q13, Q14, or Q15 shorted Q16 or D3 opened R7, R3, R6, or R8 opened C9 shorted
BUS AC LO L Will Not Go Low and/or acts erratically on power-on/power-off	Q13, Q14, or Q16 opened Q15 or D3 shorted R12, R13, R7, or R10 opened
BUS DC LO L Will Not Go High	Q19, Q20, or Q18 shorted Q17 or D3 opened R7, R2, or R6 opened C9 shorted
BUS DC LO L Will Not Go Low	Q19, Q20, of Q17 opened Q17 or D3 opened R7, R3, or R6 opened C9 shorted

*These causes make the crowbar fire, which in turn, blows the appropriate fuse.

Table 16-1 (Cont)
Troubleshooting Chart

Problem	Cause
BUS DC LO L Will Not Go Low and/or acts erratically on power-on/power-off	Q19, Q20, or Q17 opened Q18 or D3 shorted R9, R10, R11, or R8 opened
No LTC L Signal	R55 opened D13 shorted
LTC L Going Too High	D13 opened

16.5 PARTS IDENTIFICATION

Parts identification for the power supply is provided in the *Engineering Drawing Manual.* This includes the assembly drawings with associated parts lists, which list the respective unit parts, their part designation, and their DEC part numbers. These drawings and the respective drawing numbers are as follows:

a. Power Supply Chassis: E-1A-5309816-0-0

b. Power Control Board 115V: C-IA-5409824-0-0
230V: C-IA-5409825-0-0

c. DC Regulator Module: E-IA-5409728-0-0
D-CS-5409728-0-1 (schematic)

d. Power Supply Assembly and Fan: D-AD-7003731-0-0

e. AC Input Box Assembly: D-UA-H400-0-0

f. Line Set 115 Vac 7A: C-UA-BC05H-0-0
230 Vac 5A: C-UA-BC05J-0-0

PART 5
10-½ INCH MOUNTING BOX AND POWER SYSTEM

Part 5 discusses the following PDP-11/05 and PDP-11/10 Computer models:

Model NC-115 V, 47–63 Hz
Model ND-230 V, 47–63 Hz

These models are packaged in a 10-1/2 in. high mounting box. The prewired backplane can accommodate 16K of core memory and the computers are normally supplied with 8K of core memory installed. Part 5 describes only the 10-1/2 in. mounting box and power system. These items are different from the corresponding items that are used in the 5-1/4 in. high models.

Chapters of Part 5 include:

Chapter 17 Mounting Box
Chapter 18 Unpacking and Installation
Chapter 19 Power System

CHAPTER 17
MOUNTING BOX

17.1 INTRODUCTION

This chapter contains a detailed description of the mounting box (or chassis assembly) used for the PDP-11/05, 11/10 Models NC and ND. The same mounting box is used for both models except for the ac power line set which is wired for 115 V, 47–63 Hz for model NC and 230 V, 47–63 Hz for model ND.

17.2 OVERALL MECHANICAL DESCRIPTION

Figure 17-1 shows the PDP-11/05-NC Computer mounted in a cabinet. The console and top decorative panel (bezel) are attached to the mounting box with four screws each that are inserted from the rear side of the console and panel. The lower filler strip is similarly installed with two screws. The mounting screws are located along the vertical sides and are accessible when the computer is extended from the cabinet.

Figure 17-2 shows the computer fully extended from the rack and locked in the front down 90° position. The top and bottom mounting box covers have been removed. The power supply cover has been removed also. The top and bottom mounting box covers are each held in place with four Phillips pan-head screws (#6-32 X 0.37 in. long) and four #6 lock washers. The power supply cover is held in place with four Phillips pan-head screws (#10-32 X 0.31 in. long) and four #10 lock washers.

The interior of the mounting box is divided into three compartments. The smallest one extends partially across the front and contains the power distribution board and two fans for cooling the modules.

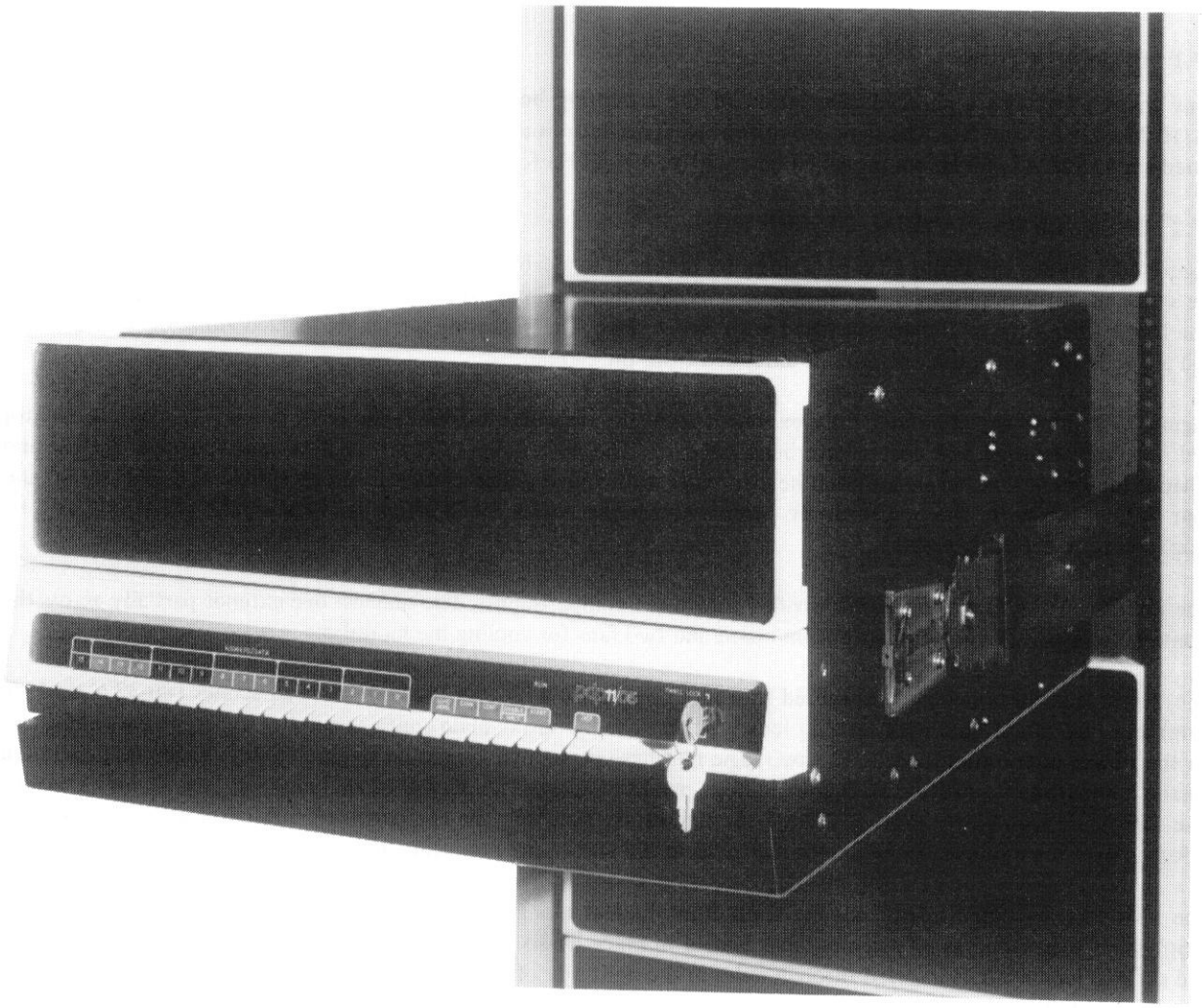
The power distribution board is secured to a mounting plate with two Phillips pan-head screws (#6-32 X 0.81 in. long) and two #6-32 nuts with integral lock washers. The mounting plate contains cutouts to accept the connectors on the power distribution board. The two logic fans have protective screens on the intake side. Each fan is mounted on the compartment partition with four Phillips pan-head screws (#6-32 X 0.62 in. long) and four #6 lock washers. The screws are secured by captive nuts on the fan. Intake air enters the compartment through slots on the left side, is forced over the modules, and exits through slots in the rear of the mounting box.

The next largest compartment extends from front to rear along the right side. This section contains the power supply that is installed as an assembly and is held in place by six Phillips pan-head screws (#10-32 X 0.31 in. long) and six #10 lock washers inserted through holes in the right side of the mounting box into nuts that are integral with the power supply chassis.

The largest compartment contains the pre-wired backplane, modules, and module guides. The basic computer contains a standard pre-wired 9-slot backplane installed pin side down next to the power supply. It is secured to both the front and rear mounting brackets by two Phillips pan-head screws (#10-32 X 1 in. long) and two #10 lock washers each that are inserted from the bottom through holes in the backplane frame (Figure 17-3). There is enough space to install one additional 9-slot backplane and one 4-slot backplane or three 4-slot backplanes.

Two rows of module guides are installed on mounting box brackets at the front and rear of the backplane compartment. The bottom row is slotted to guide the module into the slot for installation. The top row is slotted for the same reason but it also contains a steel rod that is circular in cross section. This rod engages the slotted arm of the pivoted handles on the hex-width module to provide the mechanical advantage required to properly seat and unseat the module.

The line set is attached to the rear of the mounting box (Figure 17-4) with two Phillips pan-head screws (#6-32 X 0.19 in. long). Space is available in the rear of the mounting box for cable access. Three cable retainers are mounted on a bracket on the rear of the mounting box.



6601-2

Figure 17-1 PDP-11/05 NC Computer Mounted In Cabinet

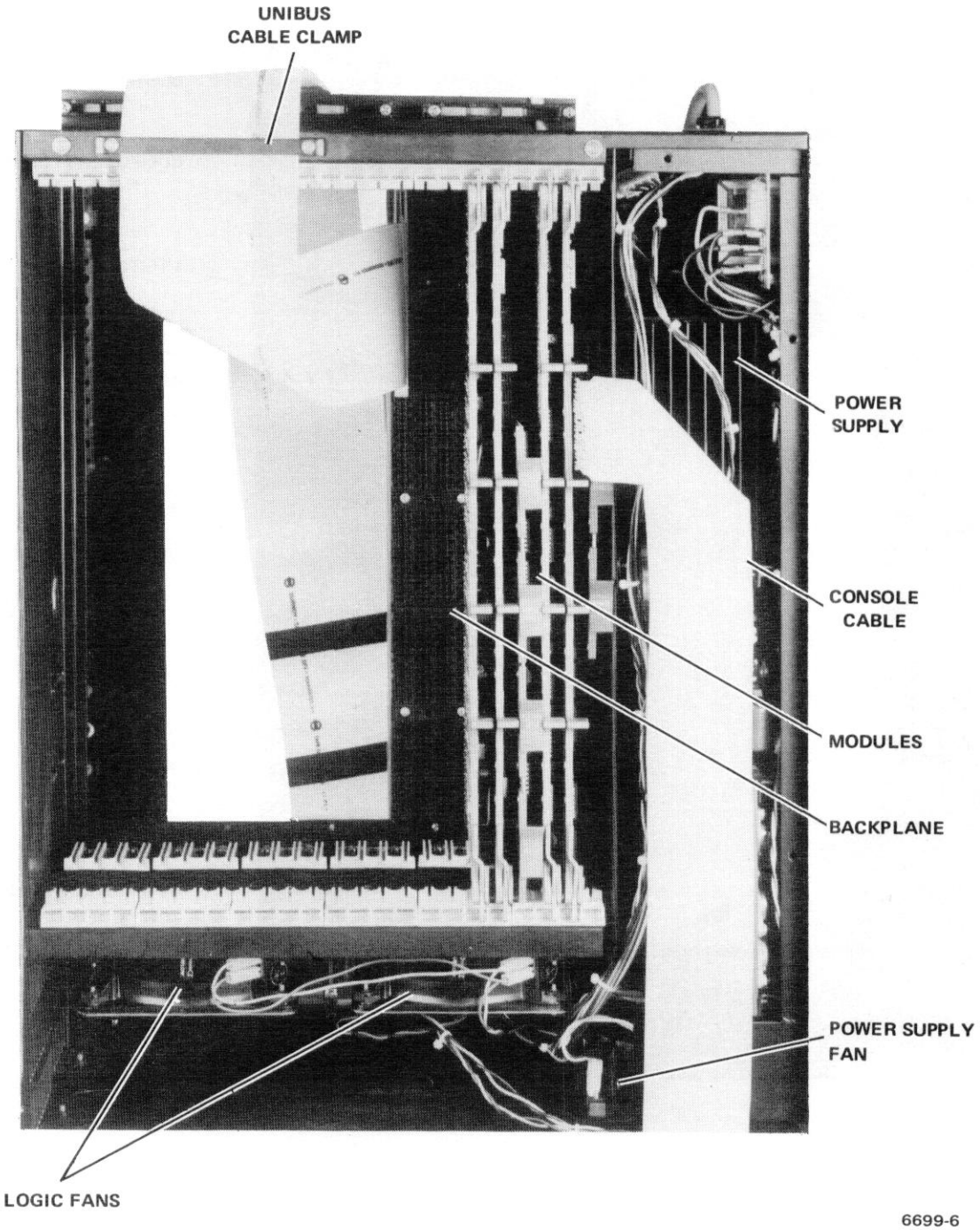


Figure 17-2 PDP-11/05 NC Computer Extended and Locked In Front Down 90° Position

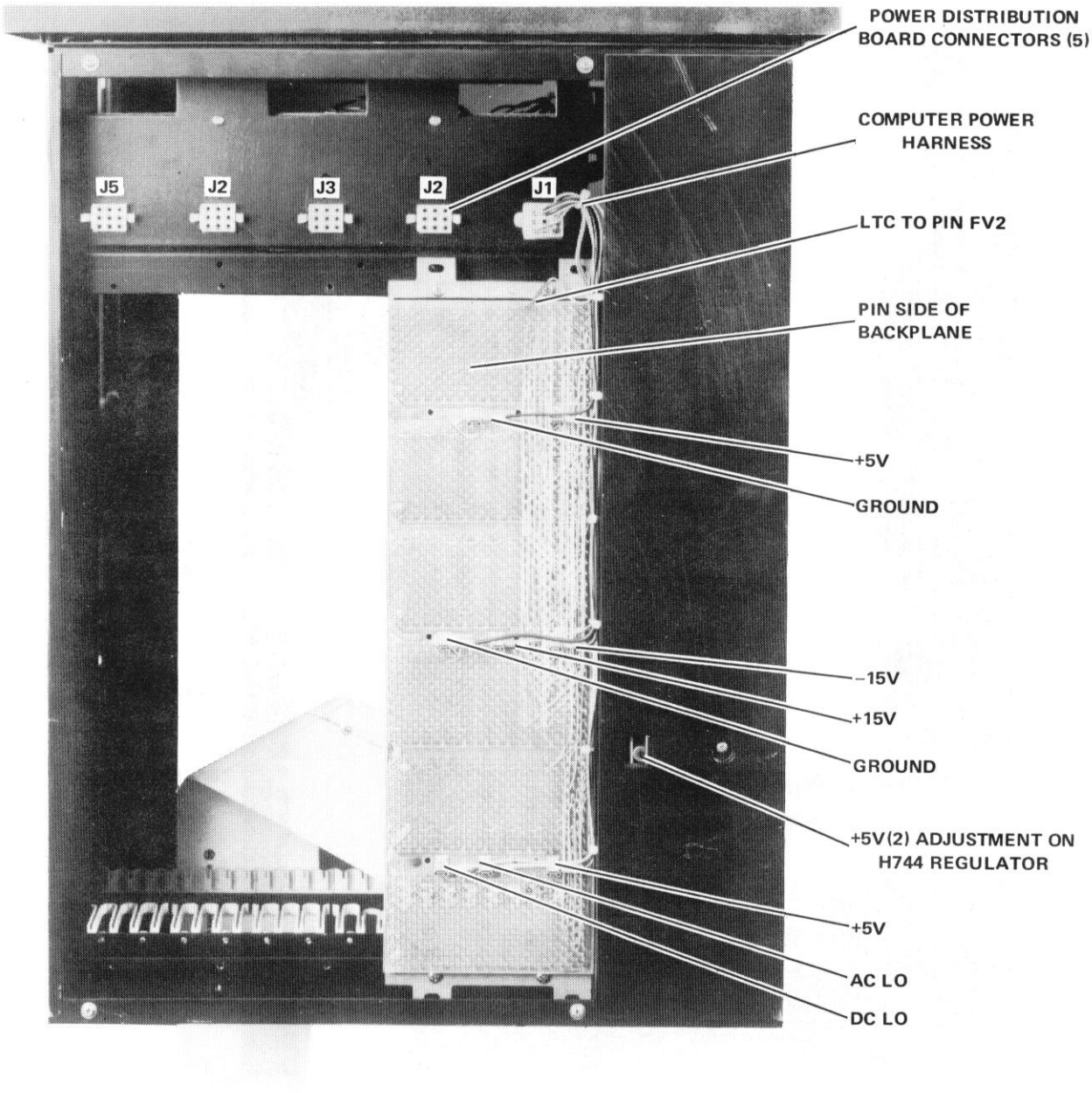


Figure 17-3 PDP-11/05 NC Computer Extended and Locked In Front Up 90° Position

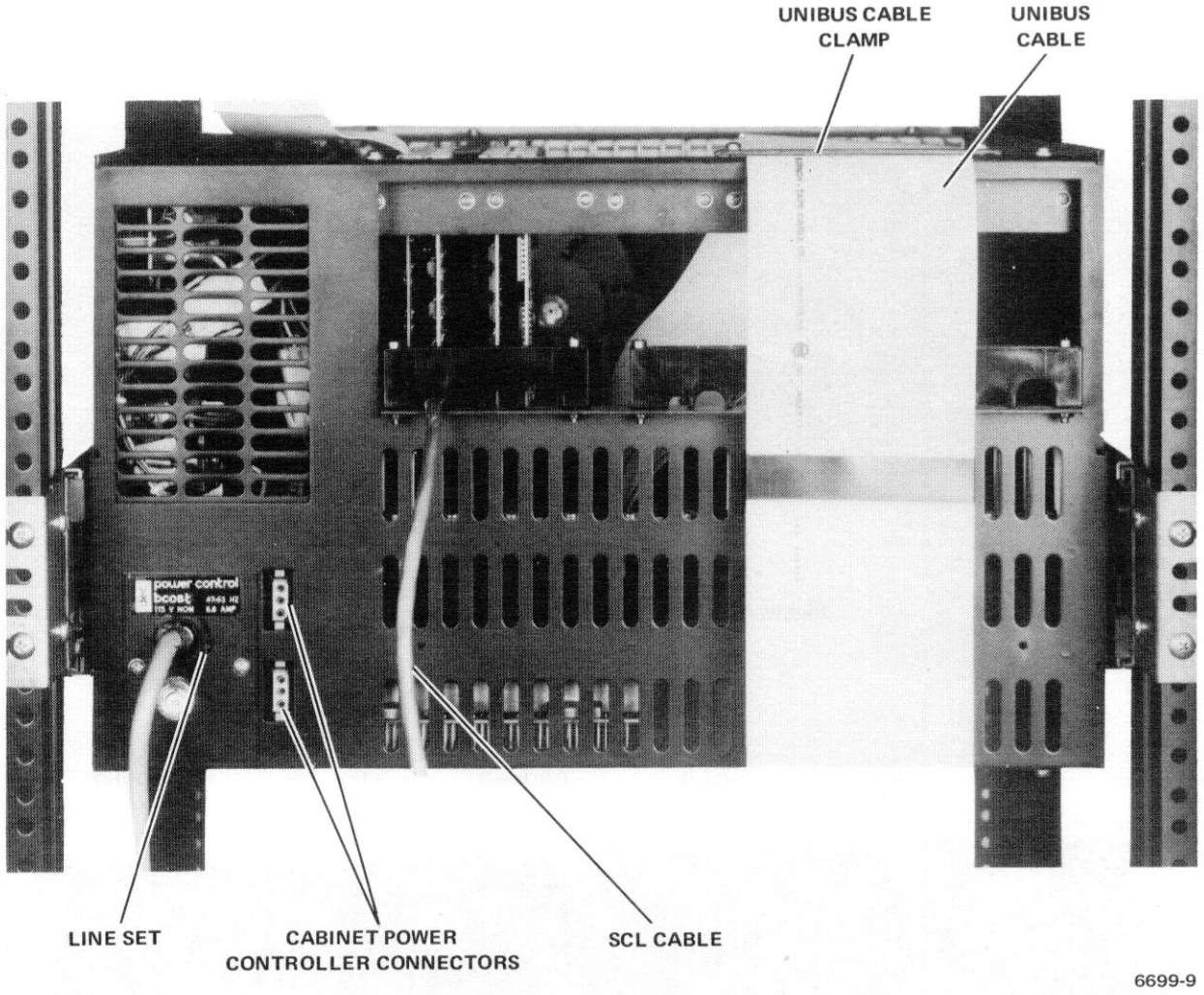
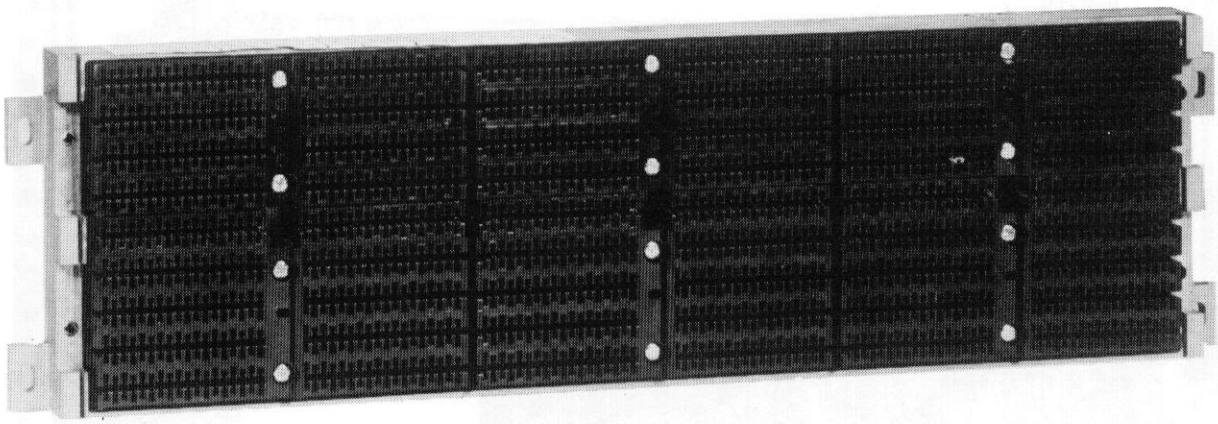


Figure 17-4 PDP-11/05 NC Computer, Rear View

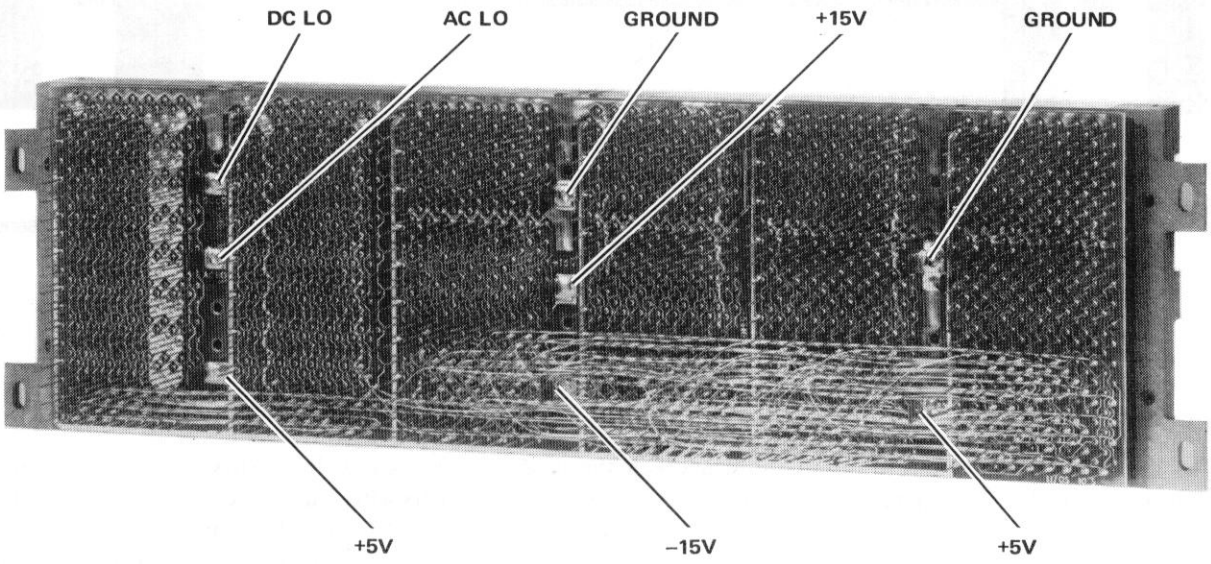
17.3 BACKPLANE

The backplane is the connector assembly into which the modules are plugged. It consists of a group of molded connectors attached to a metal frame (Figure 17-5). One side provides slots with finger type contacts into which the modules are inserted. These contacts terminate in wire wrap pins on the other side of the backplane. The pins are inserted through and soldered to a printed circuit board that is part of the backplane. This board provides most backplane interconnections and the remaining interconnections are made by wire wrapping the pins (Figure 17-6). The printed circuit board also contains eight Faston tabs that mate with Faston connectors on the processor power distribution cable. This cable provides power, ground, and sensing signals from the power supply to the backplane. The cable also contains a slip-on connector that sends the line time clock (LTC) signal from the power supply to backplane pin F03V2.



6699-12

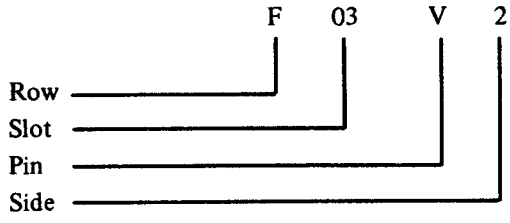
Figure 17-5 Connector Side of Backplane



6699-3

Figure 17-6 Pin Side of Backplane

Figure 17-7 shows the backplane pin layout and method of identification. The slots are numbered 1 through 9 and the rows are lettered A through F. Each row is pinned to accommodate a single-height double-sided module edge-connector. The backplane accepts single, double, quad, and hex modules. A backplane pin is identified as follows:



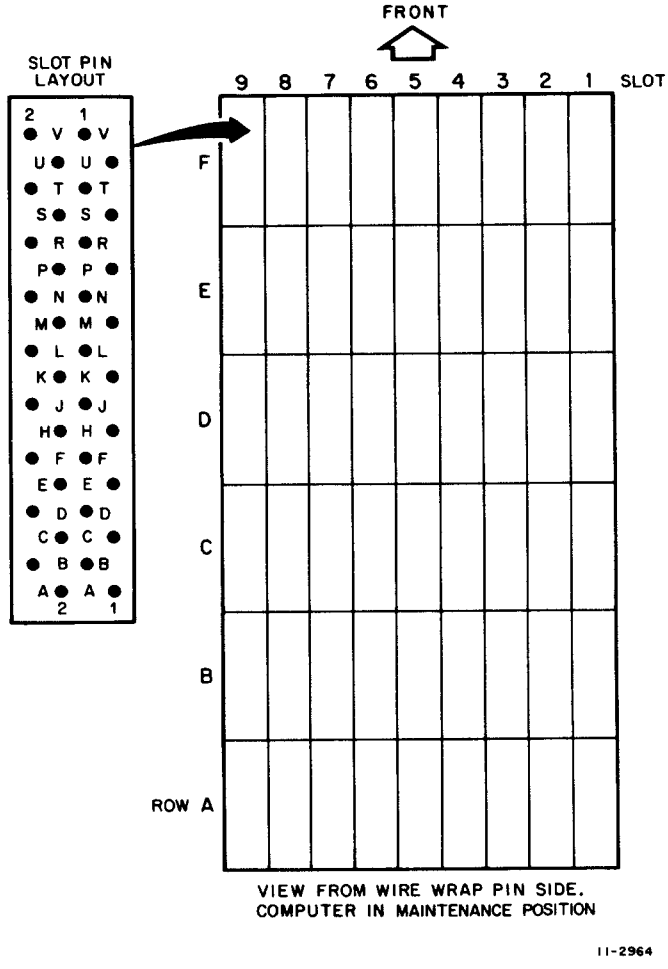
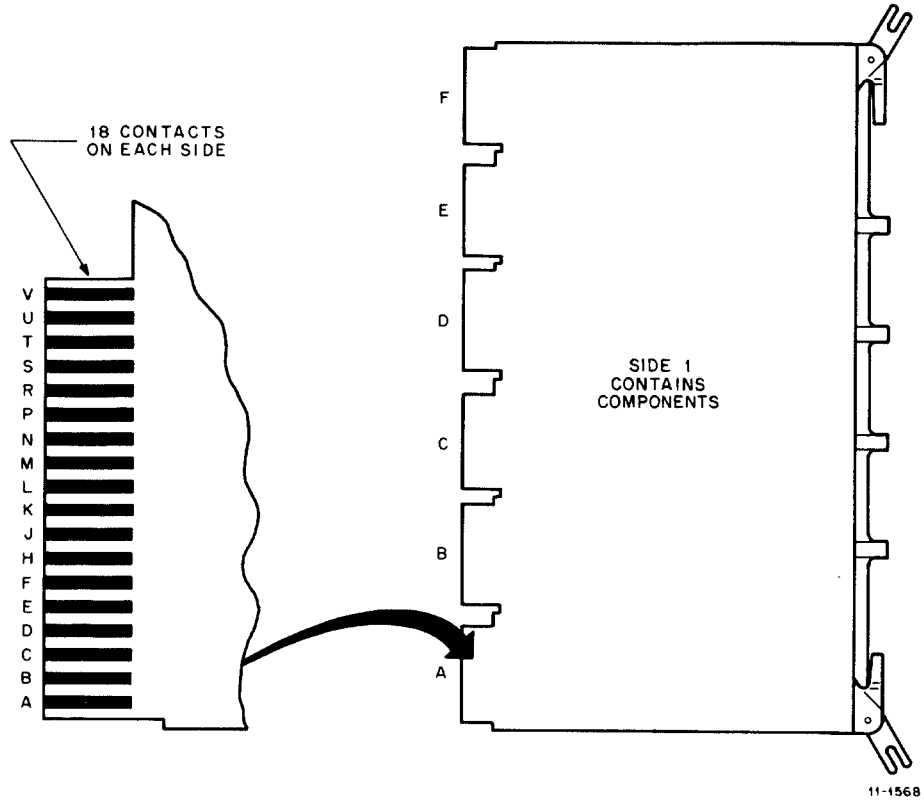


Figure 17-7 Computer Backplane Connector and Pin Designations

Each module connector contains finger contacts on each side. Module contact designations are shown in Figure 17-8.

The backplane is pre-wired for the configuration shown in Figure 17-9. If an additional backplane is installed to accommodate additional memory or options, the M930 Unibus Terminator in slot A9-B9 must be removed and installed in the appropriate slot of the added backplane. In place of the M930 removed from slot A9-B9, an M920 Unibus Jumper module is installed to connect the Unibus signals to the added backplane. The M9970 Cable Connector module in slot C1-D1 contains a 40-pin Berg connector that accepts the connector on the serial communications line cable, which is used for the ASR-33, VT05, and serial model of the LA30. Slot A1-B1 is wired for a DF11 Communications Line Adapter that provides signal conditioning for communications devices using signals that are not TTL compatible. The DF11 works with the serial communications line interface so that when it is installed, the M9970 module is not used. Slots E1 and F1 are wired for the KM11 Maintenance modules that are used during troubleshooting operations. The core memory modules must be installed in the designated slots (Figure 17-9), but they are interchangeable.



NOTES:

1. Side 1 is component side.
2. Each side contains 18 contacts that are designated A-V (omitting G,I,O,Q,W,X,Y,Z)
3. A complete designation contains a connector letter prefix, contact letter, and side suffix number. for example: AD2

Figure 17-8 Module Contact Designations

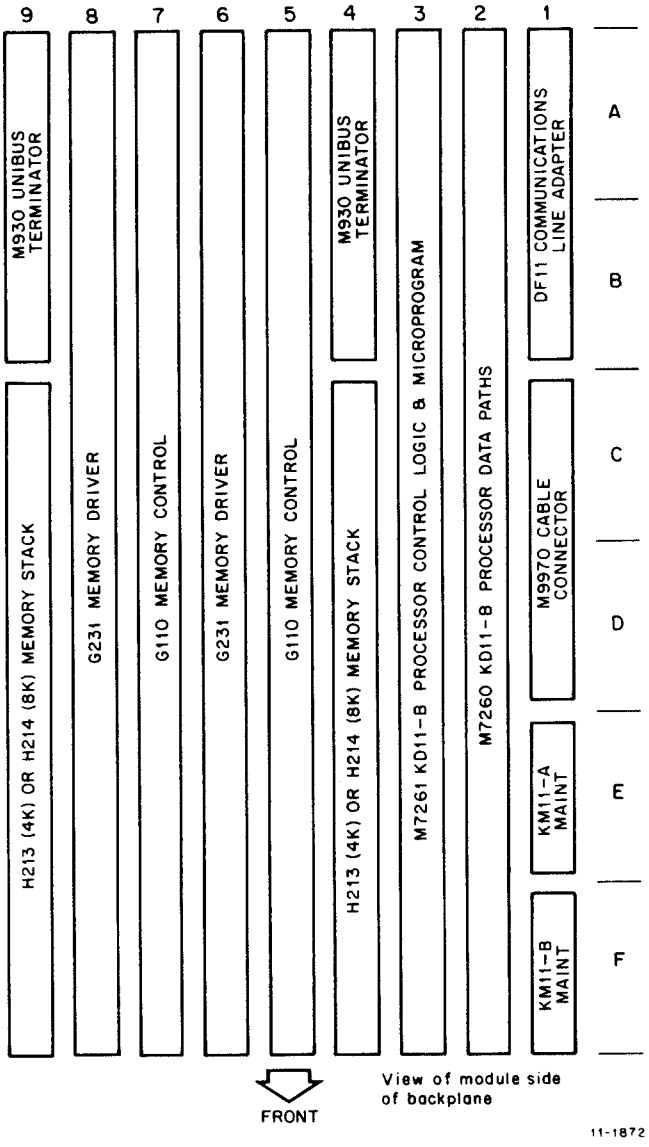


Figure 17-9 Module Utilization Diagram

17.4 POWER SYSTEM

The power system consists of the H750 power supply, BC05T/U line set, power supply wiring harness, power distribution wiring harness and board, and processor power harness.

The H750 Power Supply converts 115 V or 230 V, 47–63 Hz line voltage to regulated +5 V, +15 V and -15 V for the computer. The power supply also generates BUS AC LO L and BUS DC LO L, which are the power fail early warning signals and LTC L which is the real-time clock synchronizing signal.

The line set provides ac line power to the processor: BC05T is used for 115 V and BC05U is used for 230 V.

The power harnesses and distribution board interconnect the power supply, line set, cooling fans, and backplane.

A detailed discussion of the power system is given in Chapter 19.

CHAPTER 18
UNPACKING AND INSTALLATION

18.1 INTRODUCTION

This chapter provides information on the unpacking and installation of the computer. Information on installation certification and warranty service is also included.

18.2 UNPACKING

The computer is shipped ready to operate in a protective box (Figure 18-1) or mounted in a 19-in. cabinet. Remove the computer from the box and visually inspect for damage. Save the shipping carton and packaging materials in case it is necessary to return the computer for service. The slide mounts are attached to the computer, but the mounting screws are packed in a bag placed in the shipping container. Two console keys and a serial communications line (SCL) cable are also included. The keys are attached to the line cord at the rear of the computer. The standard SCL cable (70-08360) has a 40-pin Berg connector on one end that mates with the M9970 Cable Connector module. The other end has a Mate-N-Lok connector that mates to the one used on the LA30 DECwriter (serial model), DEC VT05 Alphanumeric CRT Display Terminal, and Teletype® Model 33 ASR. If the DF11 Communications Line Adapter is used instead of the M9970 module, the appropriate cable is included.

A computer shipped in a cabinet is locked in place to prevent movement during shipment. A shipping bracket is mounted on the back of the cabinet. The heads of two T-bolts are inserted in the cooling slots in the rear of the computer mounting box, and the heads are turned 90° so that they cannot be withdrawn. The bolt bodies protrude through holes in the shipping bracket and are secured to it by two nuts. Remove and retain the T-bolts and nuts for re-use if the cabinet is to be shipped or moved any distance.

18.3 INSTALLATION IN A CABINET

The slide assembly is installed on the computer. Unlock the slide release and remove the outer slide from each side of the computer. These are the fixed portions of the slide assembly and are mounted in the cabinets as follows.

The front of the fixed slide has an integral bracket and is mounted in the cabinet with two screws that are secured with captive nuts (Tinnerman nuts). The rear of the fixed slide is attached to a separate L-shaped bracket with two screws and nuts. The bracket is attached to the cabinet with two screws that are secured with captive nuts. Mount the fixed slides equidistant from and parallel to the floor.

Lift the computer and slide it carefully into the fixed guides until the slide release engages. Unlock the slide release and push the computer fully into the cabinet. Extend the computer enough to allow access to the front mounting screws. Slightly loosen the front and rear slide mounting screws and slide the computer back and forth. This allows the slides to assume a position that causes minimum binding. Retighten mounting screws.

® Teletype is a registered trademark of Teletype Corporation.

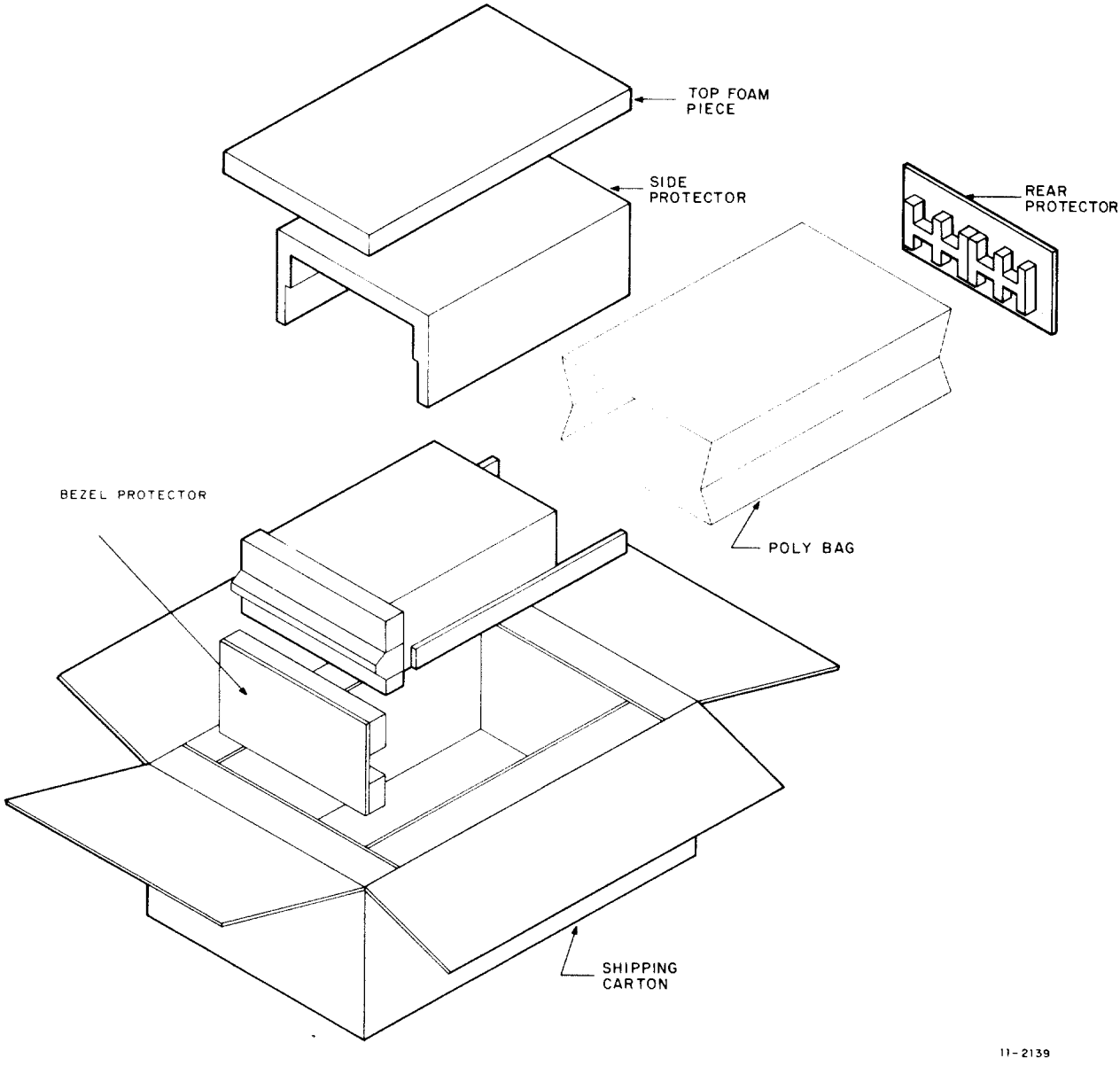


Figure 18-1 Computer Packaging

18.4 INSTALLATION OF OPTIONS AND CABLES

The basic computer is shipped with a 9-slot backplane that accommodates the processor and 8K or 16K of core memory. Enough room remains to install three 4-slot backplanes or one 9-slot and one 4-slot backplane.

If options are purchased with the computer, they are installed in the mounting box, space permitting. Adjacent backplanes are interconnected with an M920 Unibus Jumper module.

18.4.1 Installing Options on Site

Remove the mounting box top and bottom covers. From the top, place the backplanes next to one another with connector row A at the rear of the box. From the bottom, secure the backplane to the mounting flange at the front and rear using four screws for the 9-slot version and two screws for the 4-slot version.

For each option, a power harness is used to connect the backplane to the power distribution board. All cables use identical Mate-N-Lok connectors to connect to the power distribution board. The other end of the cable terminates in Faston connectors or in a cable card, depending on the type of backplane. Faston connectors are used for a backplane that has its power connections brought out to Faston tabs on the pin side. Refer to the power harness drawing to identify the Faston connectors on the cable and slip them over the tabs on the backplane which are identified on the etched surface of the backplane.

If the backplane does not use Faston tabs, the other end of the power harness terminates in a cable card. Refer to the module utilization drawing for the option and insert the cable card in the designated slot in the connector side of the backplane.

The five connectors on the power distribution board are J1–J5, with J1 next to the power supply. Normally, the processor backplane is connected to J1, and J2 is not used. If this mounting box is used as an expansion box, J2 can be used because it is possible to install five 4-slot backplanes in an extension box.

If an MF11-L Memory is to be added, place it next to the processor backplane. Connect the MF11-L power harness (70-09206) to J3 on the power distribution board. If another 4-slot backplane is to be added, the box would be filled and the power harness for this backplane should be connected to J5. Connector J4 is not used because the MF11-L backplane takes the space of two 4-slot backplanes.

If three 4-slot backplanes are to be added, connect them to J3, J4, and J5. See Table 3-2 for option power harness part numbers.

CAUTION

1. **Memory interleaving is not allowed in the PDP-11/05.**

2. **MM11-E and F Memories must not be installed in the PDP-11/05 mounting box. Neither the H750 Power Supply in the PDP-11/05 nor the MM11-E and F Memories contain the DC LO circuit that cuts off -15 V to the memory during a power interruption to avoid destruction of store data. These memories must be installed in a box that is powered by an H720 Power Supply containing the DC LO circuit.**

   The MM11-K and L Memories that are installed in the PDP-11/05 mounting box contain the DC LO circuit.

After the options are installed, use M920 Unibus Jumper modules to distribute the Unibus signals to all backplanes. Insert an M930 Unibus Terminator module in slots A4-B4 of the last backplane, if it is the last device connected to the processor.

A BC11-A Unibus cable is used to connect devices in another box to the processor. If the box contains only the processor backplane, install the Unibus cable rather than the M930 Terminator in slots A9-B9. If other options have been added, install the Unibus cable rather than the M930 Terminator in slots A4-B4 of the last backplane. Secure the Unibus cable in the strain relief clamp on the top rear surface of the mounting box (Figure 17-4). Remove the two screws that hold the Unibus cable clamp to the box. Place the cable between the box and the clamp, install the screws, and tighten loosely. Plug the cable into the backplane, leaving some slack, and tighten the screws.

Three strain relief clamps are provided on the top rear surface of the mounting box for I/O device cables.

18.4.2 Connecting the Serial Communications Device to the Processor

The 70-08360 SCL cable contains an 8-pin Mate-N-Lok connector on one end that mates with the cable on the serial communications device (Figure 18-2). The other end contains a 40-pin Berg female connector that mates with a 40-pin Berg male connector on the M9970 Cable Card that is inserted in slots C1-D1 in the computer backplane. The signals are wired, via the pin side of the backplane, to the M7260 Data Paths module. Table 18-1 contains pin and signal designations at these points and a description of each signal. Figure 18-2 shows the 70-08360 cable and Berg connector on the M9970. Connect the serial communications device (ASR 33, VT05, etc.) to the processor as follows:

1. Remove the M9970 Connector module from backplane slots C1-D1.

2. Plug the Berg connector on the 70-08360 SCL cable (supplied with the computer) into the Berg connector on the M9970.

3. Insert the M9970 into backplane slots C1-D1.

4. Connect the Mate-N-Lok connector on the SCL cable to the Mate-N-Lok connector on the cable that is attached to the serial communications device.

5. Place the SCL cable in one of the strain relief clamps.

18.4.3 Console Cable

Console cable BC08R-03 is a 3-ft flat cable with 40-pin female Berg connectors on each end. Table 18-2 lists the pin and signal designations for the console cable.

18.4.4 Unibus Cable/Jumper

Table 18-3 lists the pin and signal designations for the Unibus BC11A Cable and Unibus M920 Jumper.

18.5 AC POWER SUPPLY CONNECTION

Computers designed for use on 115-Vac circuits are equipped with a 3-prong connector, which, when inserted into a properly wired 115-Vac outlet, grounds the case of the computer. It is unsafe to operate the computer unless the case is grounded since normal leakage current from the power supply flows into metal parts of the chassis.

If the integrity of the ground circuit is questionable, the user is advised to measure the potential between the computer case and a known ground with an ac voltmeter.

18.5.1 Connecting to Voltages Other than 115 V

The computer operates at voltages ranging from 95 V to 135 V and from 190 V to 270 V (47 Hz – 63 Hz), providing the proper line set is attached to the computer. The plug is part of the line set. The plug configuration and specifications are shown in Figure 18-3.

On installation outside of the United States or where the National Electrical Code does not govern building wiring, the user is advised to proceed with caution.

18.5.2 Quality of AC Power Source

Computer systems consisting of the processor, memory, and peripherals are often sensitive to the interference present on some ac power lines. If a computer system is to be installed in an electrically noisy environment, it may be necessary to condition the ac power line. DEC Field Service Engineers can assist customers in determining if their ac line is satisfactory.

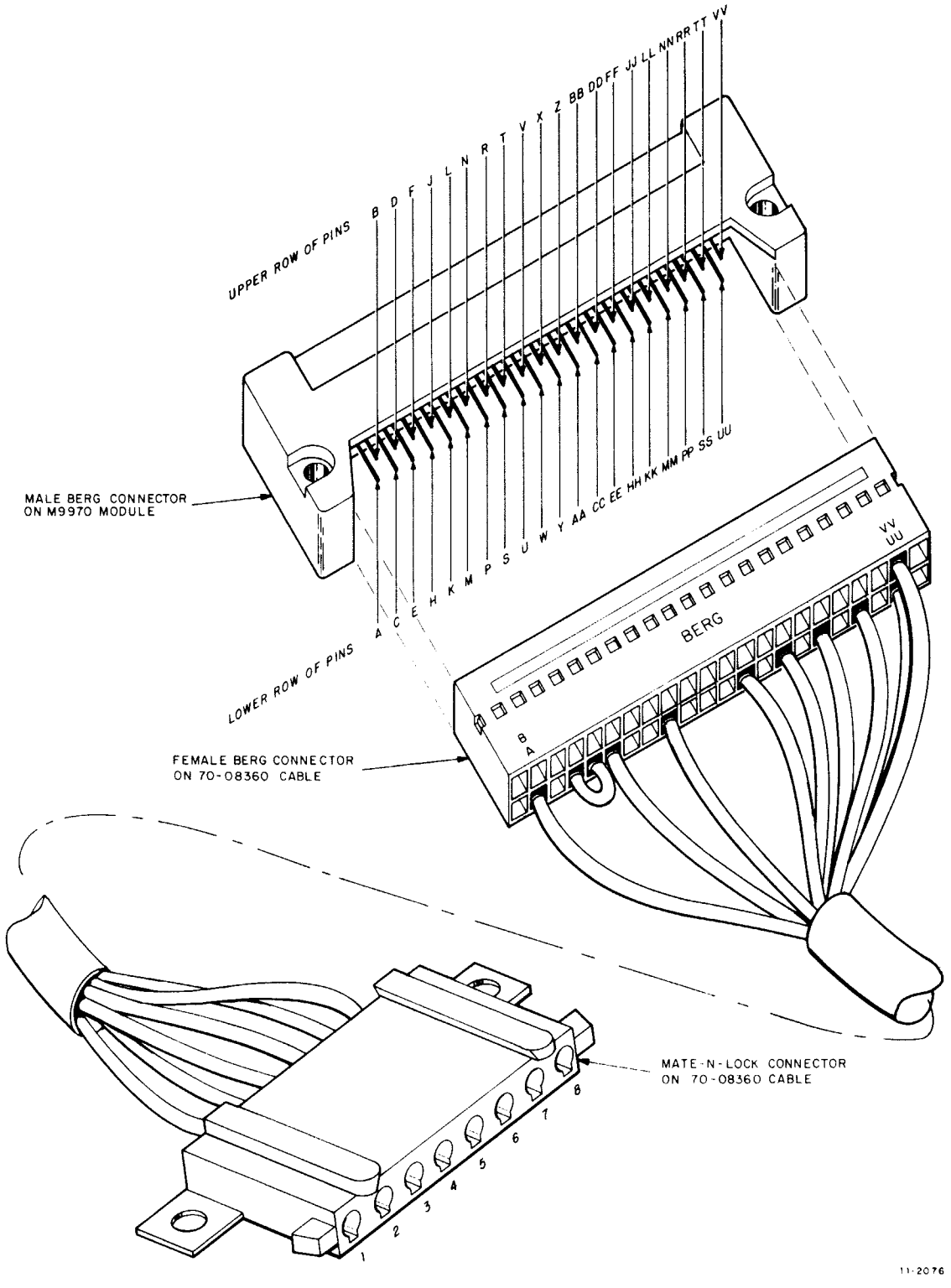


Figure 18-2 SCL Cable 70-08360

Table 18-1
SCL Interface Pin and Signal Designations

70-08360 CABLE SIGNAL NAME	MATE-N-LOK PIN ON 70-08360 CABLE	BERG PIN ON 70-08360 CABLE	BERG PIN ON M9970 CABLE CARD	SIGNAL NAME ON M7260 MODULE	M7260 PIN	SIGNAL DESCRIPTION	
SER 0 + (20 mA)	5	AA	AA	DPH SER 0 L	FE2	+20 mA SERIAL OUT (from computer)	
SER 0 – (20 mA)	2	KK	KK	DPH SER 0–15 L	FJ2	-20 mA SERIAL OUT	
SER IN + (20 mA)	7	K	K	DPH SER IN H	FN1	+20 mA SERIAL IN (to computer)	
SER IN - (20 mA)	3	S	S	DPH SI-15 L	FP1	-20 mA SERIAL IN	
READER RUN + (20 mA)	6	PP	PP	DPH RDR ENAB L	FK2	+20 mA TTY READER ENABLE	
READER RUN - (20 mA)	4	EE	EE	DPH RE -15 L	FR1	-20 mA TTY READER ENABLE	
SER 0 (TTL)	–	SS	SS	DPH SER 0 H	DF1	SERIAL DATA OUT (from computer)	NOTE 1
SER IN (TTL)	–	E	E	FS SER IN H	FM1	SERIAL DATA IN (to computer)	NOTE 1
CLK IN (TTL)	–	CC	CC	FS CLK L	FH1	EXTERNAL CLOCK INPUT FOR SCL	NOTE 1,2
CLK DISAB (TTL)	–	HH	HH	FS CLK DISAB L	FH2	DISABLE LINE FOR INTERNAL SCL CLOCK	NOTE 1,3
20 mA INTERLOCK	–	H,E	–	–	–	NOT USED ON THIS INTERFACE	
+5 V	–	TT	TT	–	–	+5 V POWER AVAILABLE EXTERNALLY	
+15 V	–	U	U	–	–	+15 V POWER AVAILABLE EXTERNALLY	
GROUND	–	A,B,UU,VV	A,B,UU,VV	–	–	LOGIC GROUND	

NOTE 1: These signals are TTL compatible.

NOTE 2: Externally supplied SCL CLOCK must be 16 times desired buad rate (max. baud rate is 10,000 baud).

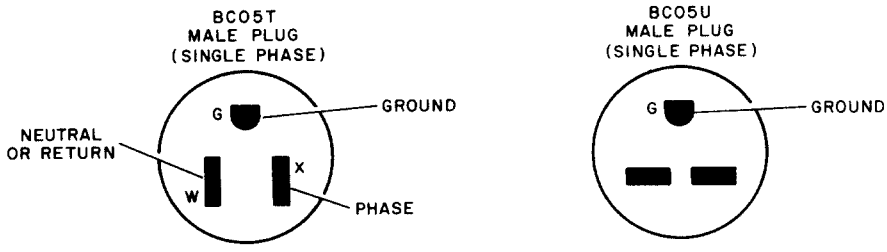
NOTE 3: This signal must be asserted low to disable internal clock if the external TTL CLOCK is to be used.

Table 18-2
BC08R-03 Console Cable Pin and Signal Designations

Designations	
Pin	**Signals**
PP	DAK H
BB	SW 15 (1) H
DD	SW 14 (1) H
FF	SW 13 (1) H
JJ	SW 12 (1) H
LL	SW 11 (1) H
NN	SW 10 (1) H
RR	SW 09 (1) H
TT	SW 08 (1) H
J	SW 07 (1) H
L	SW 06 (1) H
N	SW 05 (1) H
R	SW 04 (1) H
T	SW 03 (1) H
V	SW 02 (1) H
X	SW 01 (1) H
Z	SW 00 (1) H
HH	SCAN ADRS 01 (1) L
KK	SCAN ADRS 02 (1) L
MM	SCAN ADRS 03 (1) L
SS	SCAN ADRS 04 (1) L
CC	PUP L
C	RUN L
E	KEY LOAD ADRS (1) L
H	KEY EXAM (1) L
K	KEY CONT (1) L
M	KEY HLT ENB (1) L
P	KEY START (1) L
S	KEY DEP (1) L

Table 18-3
Unibus BC11A Cable/M920 Jumper
Pin and Signal Designations

Designation		Designation	
Pin	Signals	Pin	Signals
AA1	INIT L	BA1	BG 6 H
AA2	POWER (+5 V)	BA2	POWER (+5 V)
AB1	INTR L	BB1	BG 5 H
AB2	GROUND	BB2	GROUND
AC1	D00 L	BC1	BR 5 L
AC2	GROUND	BC2	GROUND
AD1	D02 L	BD1	GROUND
AD2	D01 L	BD2	BR 4 L
AE1	D04 L	BE1	GROUND
AE2	D03 L	BE2	BG 4 H
AF1	D06 L	BF1	AC LO L
AF2	D05 L	BF2	DC LO L
AH1	D08 L	BH1	A01 L
AH2	D07 L	BH2	A00 L
AJ1	D10 L	BJ1	A03 L
AJ2	D09 L	BJ2	A02 L
AK1	D12 L	BK1	A05 L
AK2	D11 L	BK2	A04 L
AL1	D14 L	BL1	A07 L
AL2	D13 L	BL2	A06 L
AM1	PA L	BM1	A09 L
AM2	D15 L	BM2	A08 L
AN1	GROUND	BN1	A11 L
AN2	PB L	BN2	A10 L
AP1	GROUND	BP1	A13 L
AP2	BBSY L	BP2	A12 L
AR1	GROUND	BR1	A15 L
AR2	SACK L	BR2	A14 L
AS1	GROUND	BS1	A17 L
AS2	NPR L	BS2	A16 L
AT1	GROUND	BT1	GROUND
AT2	BR 7 L	BT2	C1 L
AU1	NPG H	BU1	SSYN L
AU2	BR 6 L	BU2	C0 L
AV1	BG 7 H	BV1	MSYN L
AV2	GROUND	BV2	GROUND



CONNECTOR SPECIFICATIONS

MODEL NUMBER	NEMA* CONFIGURATION	DESCRIPTION	POLES	WIRES	PLUG		RECEPTACLE	
					DEC PART NO.	HUBBEL	DEC PART NO.	HUBBEL
BC05T	5-15	115V, 15AMP	2	3	90-08938	5266-C	12-05351	5262
BC05U	6-15	230V, 15 AMP	2	3	90-08853	5665-C	12-11204	5662

*ADD P SUFFIX FOR PLUG
ADD R SUFFIX FOR RECEPTACLE

11-1761

Figure 18-3 Connector Specifications for Line Set

18.6 CABINET POWER CONTROL

18.6.1 Introduction

The PDP-11/05 and PDP-11/10 Computers have provisions to allow the console switch to control the operation of the cabinet mounted 860 or 861 Power Controller.

The computer is connected to the power controller via Mate-N-Lok connector J3 or J4, each of which is part of the power supply harness (H1). These connectors are mounted on the power supply chassis and are accessible at the rear of the computer (Figure 17-4). Two connectors are provided so that other devices in the cabinet can be connected in a daisy-chain manner to the power controller. A typical cabinet power control system wiring diagram using a PDP-11/05 and one power controller is shown in Figure 18-4.

When the PDP-11/05 console switch is in the POWER or PANEL LOCK positions, the power controller is activated and power is supplied to all devices in the cabinet. In multi-cabinet systems, appropriately wired power controllers in the additional cabinets are activated when the PDP-11/05 console switch is in the POWER or PANEL LOCK positions.

The power controller provides eight switched power outlets and four unswitched outlets. The 860 controller outputs are available at two connector strips installed in the cabinet. The 861 controller outputs are installed in the controller front panel.

Functionally, both the 860 and 861 operate in the same way. A 3-wire cable is used to interconnect power controllers, computer, and other peripherals in a system. Line 1 is a POWER REQUEST, Line 2 is EMERGENCY SHUTDOWN, and Line 3 is SIGNAL RETURN (ground). Line 2 is connected to Line 3 through a thermostat, mounted on the controller. The controller LOCAL/OFF/REMOTE switch is placed in the REMOTE position for this application. Placing the PDP-11/05 console in the POWER or PANEL LOCK position, connects lines 1 and 3 which energizes the power controller and supplies ac power to the system. If an overtemperature occurs in a cabinet, the thermostat closes, connecting lines 2 and 3, and disables the switched outlets of all controllers in the system. The unswitched outlets are not affected. Refer to the *861-A,B,C Power Controller Maintenance Manual* DEC-00-H861A-A-D, for additional information.

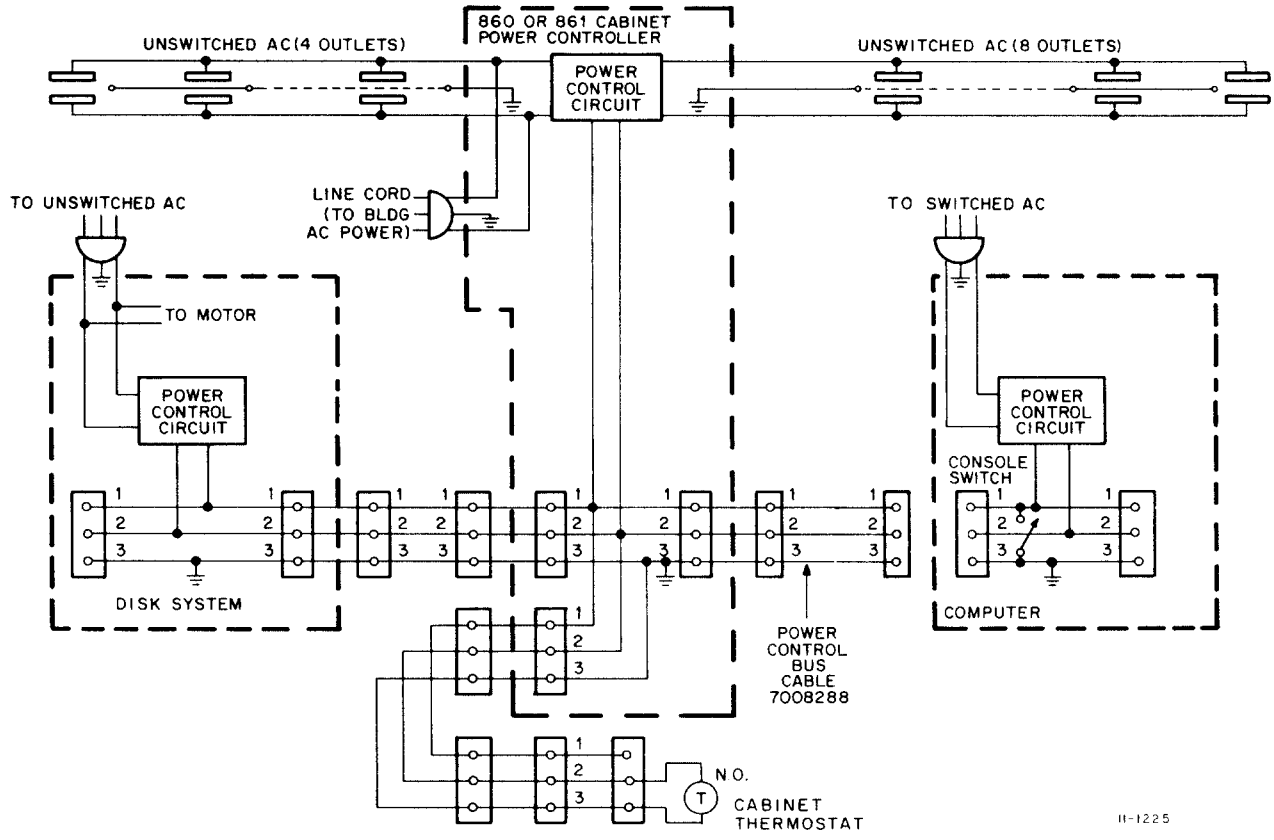


Figure 18-4 Typical Cabinet Power Control System Wiring Diagram

18.6.2 Typical Multi-Cabinet Installation

Figure 18-5 shows a typical multi-cabinet installation. Specifically, it shows the interconnection of the PDP-11/05 Computer, three power controllers, and three model H720 E/F Power Supplies in a three-cabinet system. The interconnection is identical for model 860 or 861 Power Controllers.

The 3-wire cable (7008288) that is used to interconnect the power controllers and computer allows the controllers to be operated in the local or remote mode and permits switched power to be shut off if any power controller overtemperature switch is activated.

In this example, each power controller should have its LOCAL/OFF/REMOTE switch in the REMOTE position in order to respond to the computer key switch. Placing the computer key switch in the POWER or PANEL LOCK position, with the power controller switch in the REMOTE position, energizes the controller and supplies ac power to the switched outputs. If the power controller switch is placed in the LOCAL position, ac power is supplied to the switched outputs and the computer key switch does not affect controller operation. Individual cabinets can be turned on and off using the LOCAL switch position, which is convenient during system troubleshooting. Power is supplied to the unswitched outputs in the LOCAL or REMOTE switch positions as long as the controller circuit breaker is on.

Figure 18-5 shows two methods of supplying power to options that use H720 E/F type power supplies.

The first, or local method, relates to the H720 E/F that is connected to the power controller in additional cabinet 1. The power controller interconnection cable is not used: jumper plugs 7007006-1 and 7007006-2 are installed in the two unused connectors. The ac line cord for the H720 E/F is plugged into the power controller switched ac outlet.

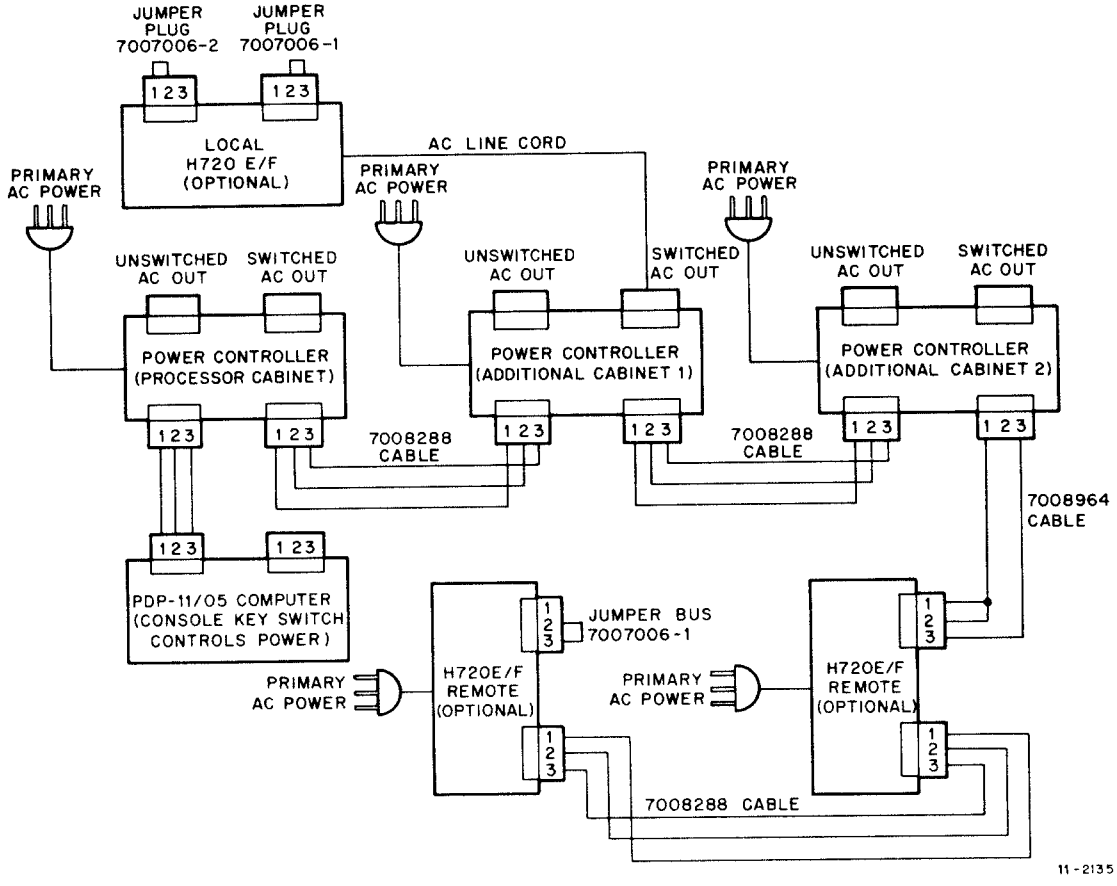


Figure 18-5 Interconnection of Power Controllers in Multi Cabinet Installation

The H720 E/F REMOTE/LOCAL switch is placed in the LOCAL position. This power supply is turned on when the computer key switch is placed in the POWER or PANEL LOCK position.

The second, or remote method, relates to the two H720 E/F Power Supplies associated with the power controller in additional cabinet 2. Both supplies are daisy-chained to the controller using the interconnecting cable. The first H720 E/F is connected to the controller with 2-wire cable 7008964. In turn, it is connected to the second H720 E/F with 3-wire cable 7008288. This power supply has jumper 7007006-1 installed in the unused connector. Both H720 E/F REMOTE/LOCAL switches are placed in the REMOTE position, and both ac power cords are plugged into wall outlets. These supplies are turned on when the computer key switch is placed in the POWER or PANEL LOCK position. Each H720 E/F can be turned on individually with the computer key switch OFF by placing the power supply switch in the LOCAL position.

18.7 INSTALLATION CERTIFICATION

Once the computer has been installed, it is strongly recommended that a system diagnostic be run to ensure that the equipment operates correctly and that installation has been properly performed. Because system configurations widely vary, no one diagnostic will completely exercise all the attached devices.

The *MAINDEC User's Manual* that comes with the diagnostic package should be consulted for the appropriate diagnostic to be run, depending upon the attached devices. The *MAINDEC User's Manual* lists the devices that each diagnostic will exercise. The three system exercisers presently available are T17 System Exerciser

(MAINDEC-11-DZQKB) for relatively small systems, General Test Program (MAINDEC-11-DZQGA) for medium to large systems, and Communications Test Program (MAINDEC-11-DZQCA) for communications-oriented systems. At least one of the above diagnostics and, if appropriate, the other two, should be used to verify system operation.

Once the diagnostic is selected, the respective diagnostic write-up should be consulted for specific operating instructions. If the user is not familiar with console operation and/or procedures for loading paper tapes, he should read Chapter 4.

18.8 WARRANTY SERVICE (DOMESTIC ONLY)

The PDP-11/05 Computer is sold with the 30 day, return-to-factory warranty. If the computer warranty period has expired or it is covered by on-site warranty, the local DEC field service office should be contacted. If the computer is still covered by the 30 day, return-to-factory warranty, and factory service is required, the following procedure should be used.

1. Call the Maynard, Massachusetts Repair Depot, Telephone 617-897-5111, X4079 or X2135.

2. The caller will receive a return authorization (RA) number that must appear on the shipping label of the returned package. Do not return equipment for repair unless it has an assigned RA number.

3. Package the computer in a shipping container equivalent to the one that it arrived in. Use the original shipping container, if possible.

4. Send the computer to the following address:

   Digital Equipment Corporation
   146 Main Street
   Maynard, Massachusetts 01754
   Attn: Depot Repair, Bldg. 8-2
   RA #XXXX

The PDP-11/10 Computer is sold with the 90 day, on-site warranty. Call the local DEC field service office if service is desired.

CHAPTER 19
POWER SYSTEM

19.1 INTRODUCTION

This chapter provides a mechanical description of the power system that consists of the H750 Power Supply, BC05T/U line set, and three wiring harnesses. A system functional description and detailed electrical interconnection diagram is included.

The regulator circuits are discussed in detail. Regulator maintenance and troubleshooting information is included also.

19.2 MECHANICAL DESCRIPTION

19.2.1 Power Supply

The power supply consists of three transformers (T1, T2, T3), dc regulator (PS1), +5 V regulator (PS2), relay (K1), diode board (PS3), terminal board (TB1), and fan mounted in a sheet metal chassis (Figures 19-1 and 19-2).

The chassis is rectangular in shape and measures approximately 22 in. long by 9-1/2 in. high by 5 in. wide. The top and left side are open and all the components are mounted on the solid bottom and right side. The main structual member is the mounting plate that is a single piece of sheet metal bent to form the right side and bottom of the chassis. Two end pieces are welded to the mounting plate. Component mounting is facilitated by threaded inserts that are installed in integral brackets and by holes in the right side and bottom of the chassis. The front cover has a cutout for the fan and holes for the fan mounting screws. The rear cover has cutouts for the line set and two Mate-N-Lok connectors. Several holes in this cover allow air to be drawn in by the fan to cool the power supply.

The power supply components are mounted as follows.

The dc regulator (PS1) is attached to six integral brackets on the side of the chassis with six Phillips pan-head screws (#6-32 X 1/2 in. long) and #6 lock washers. The regulator is installed with the heat sink facing inward. The screws pass through holes in the board and are threaded into inserts in the brackets.

The additional +5 V regulator (PS2) is attached to the side of the chassis with four Phillips pan-head screws (#4-40 X 5/16 in. long) and four #4 lock washers. The screws pass through holes in the chassis and are threaded into four standoffs (#4-40 X 3/4 in. long) that are attached to the +5 V regulator mounting bracket.

The diode board (PS3) is attached to the side of the chassis with two Phillips truss-head screws (#6-32 X 3/8 in. long) and two #6 lock washers. The screws pass through holes in the chassis and are threaded into two standoffs (#6-32 X 3/4 in. long) that are attached to the diode board.

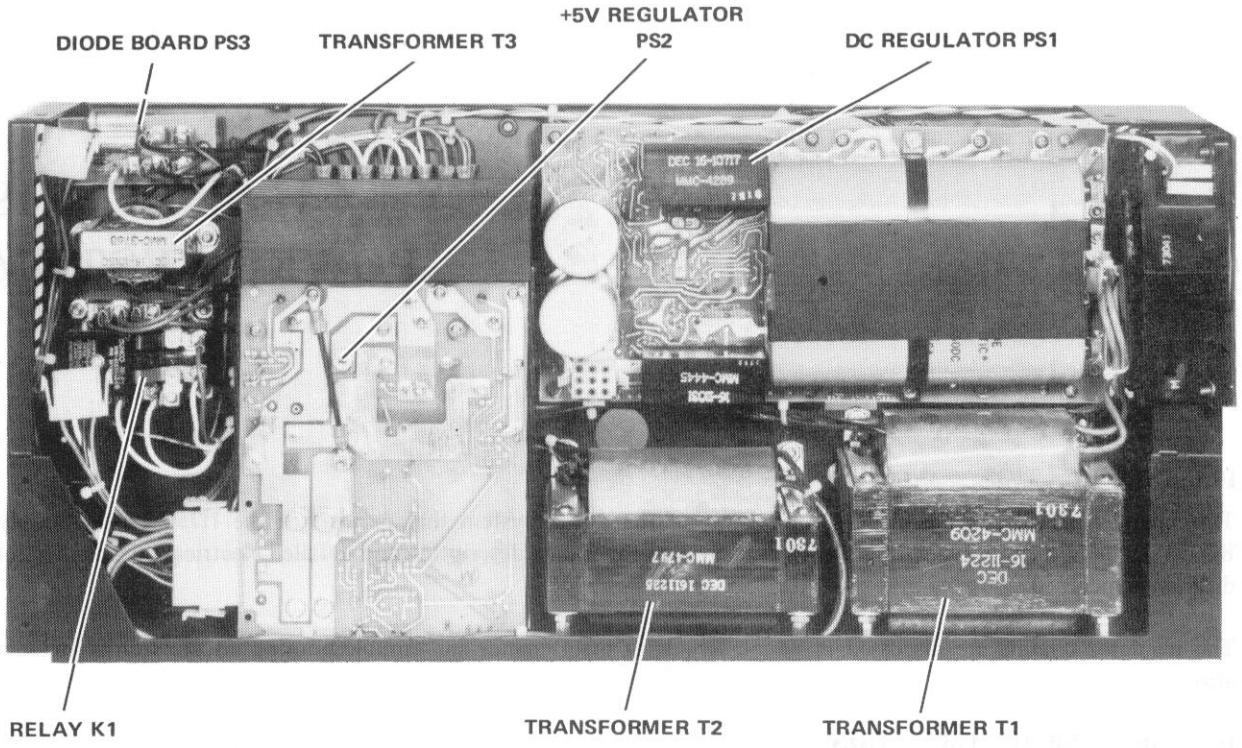


Figure 19-1 Power Supply Side View

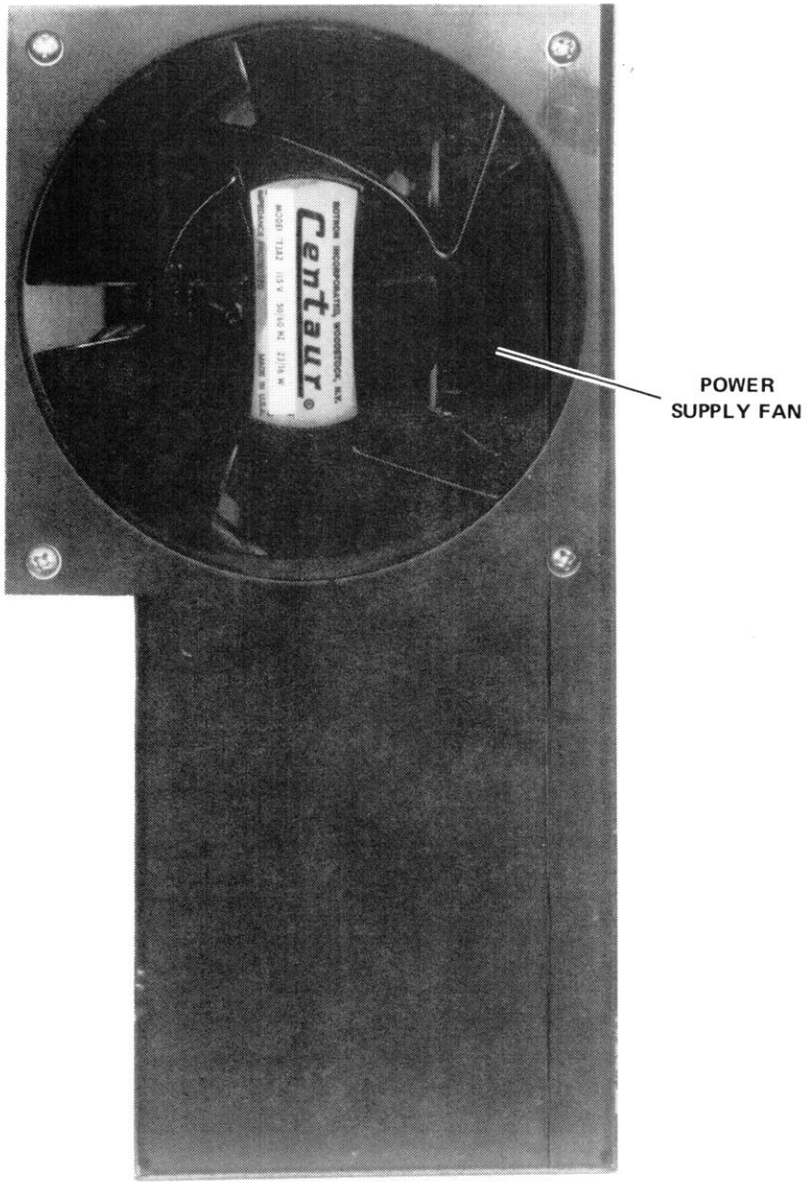
Relay K1 is attached to the side of the chassis with four Phillips truss-head screws (#8-32 X 5/8 in. long) and four #8-32 Kep nuts that have integral lock washers.

Transformers T1 and T2 are attached identically to the side and bottom of the chassis. Each transformer is attached to the bottom of the chassis by four Phillips flat-head screws (#8-32 X 1/4 in. long). The screws pass through dimpled holes in the chassis and are threaded into #8-32 standoffs that are attached to the transformer. Each transformer is attached to the side of the chassis at its top and bottom. At the top, the attachment is made with two Phillips truss-head screws (#10-32 X 7/16 in. long) that pass through holes in the chassis and transformer bracket and are secured by two #10-32 Kep nuts. These nuts are accessible inside the chassis. At the bottom, the attachment is made by two identical screws; however, they are threaded into two #10-32 U-shaped, self-retaining speed nuts (Tinnerman nuts) attached to the transformer bracket. Tinnerman nuts are used because these attaching points are not accessible from inside the chassis.

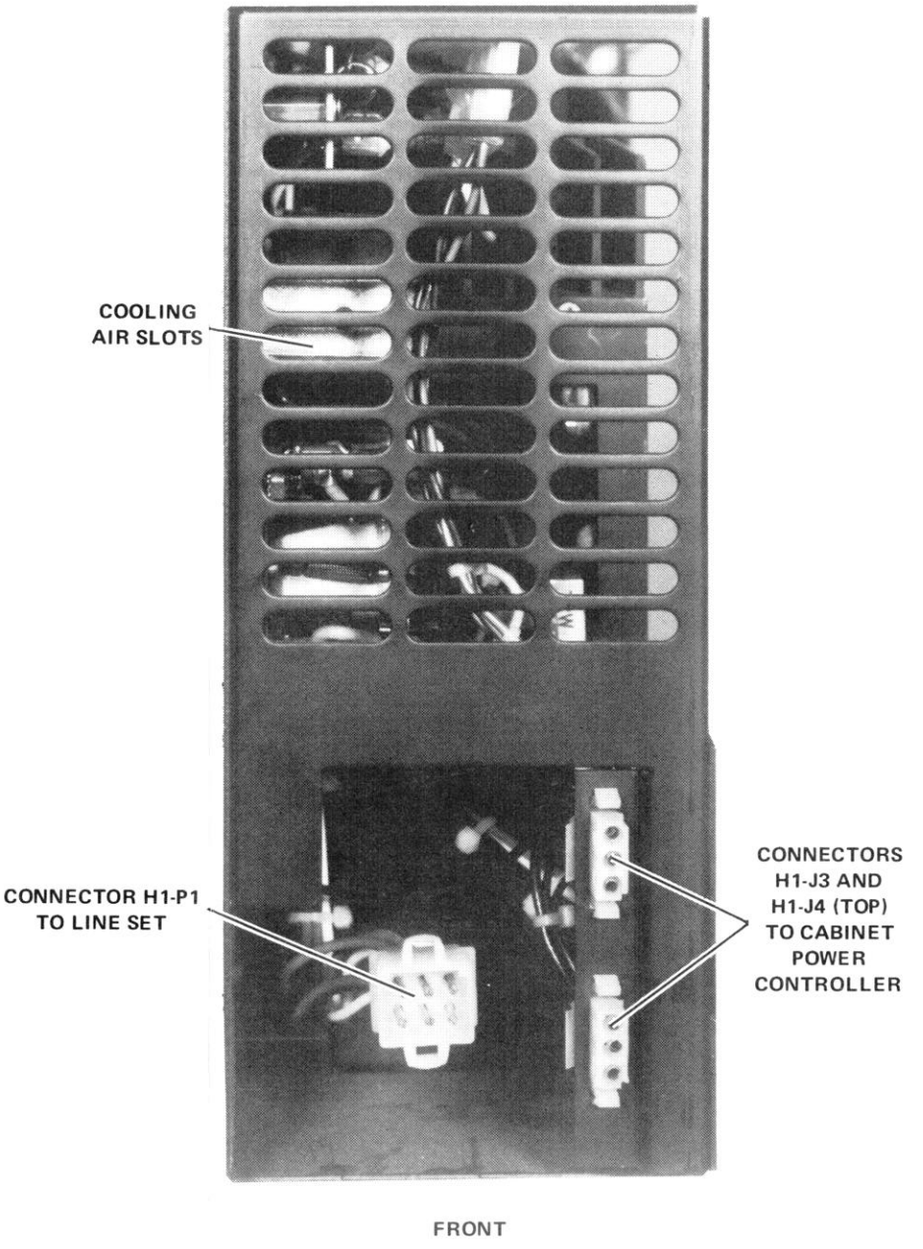
Transformer T3 is attached with two Phillips truss-head screws (#8-32 X 3/8 in. long) that pass through holes in the chassis and transformer bracket and are secured by two #8-32 Kep nuts.

Terminal block TB1 is attached to the side of the chassis with two each Phillips pan-head screws (#6-32 X 5/8 in. long), #6 lock washers, and #6-32 Kep nuts.

The fan is attached to the front end of the chassis with four Phillips pan-head screws (#6-32 X 5/8 in. long) and four #6 lock washers. The screws pass through holes in the chassis and are secured by self-retaining nuts on the fan.



6699-2



6699-5

Figure 19-2 Power Supply, Front and Rear Views

19.2.1.1 DC Regulator – The 5049728 dc regulator (Figures 19-3 and 19-4) consists of a printed circuit board, heat sink, discrete electronic components, thermostat with cable connector, ac input and dc output connectors, and attaching hardware. Table 19-1 lists the specifications for the 5409728 dc regulator.

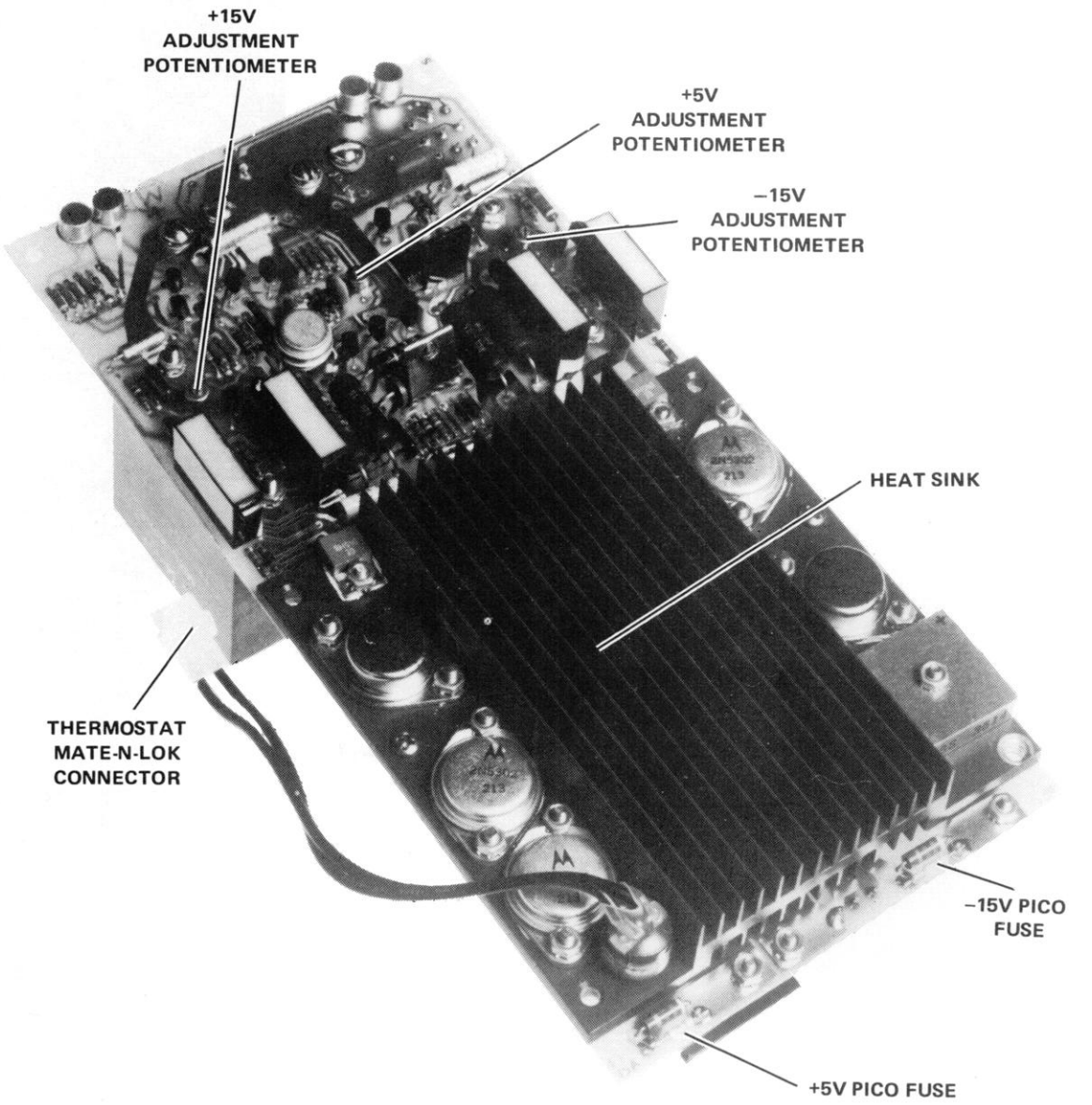


Figure 19-3 DC Regulator, Top View

Current shipments use regulator 5409728-0-0, J revision that is discussed in this manual. Earlier revisions differ in component values and current ratings. Engineering drawings applicable to the module used are shipped with the equipment. These drawings include a schematic of the dc regulator module that shows component values and part numbers.

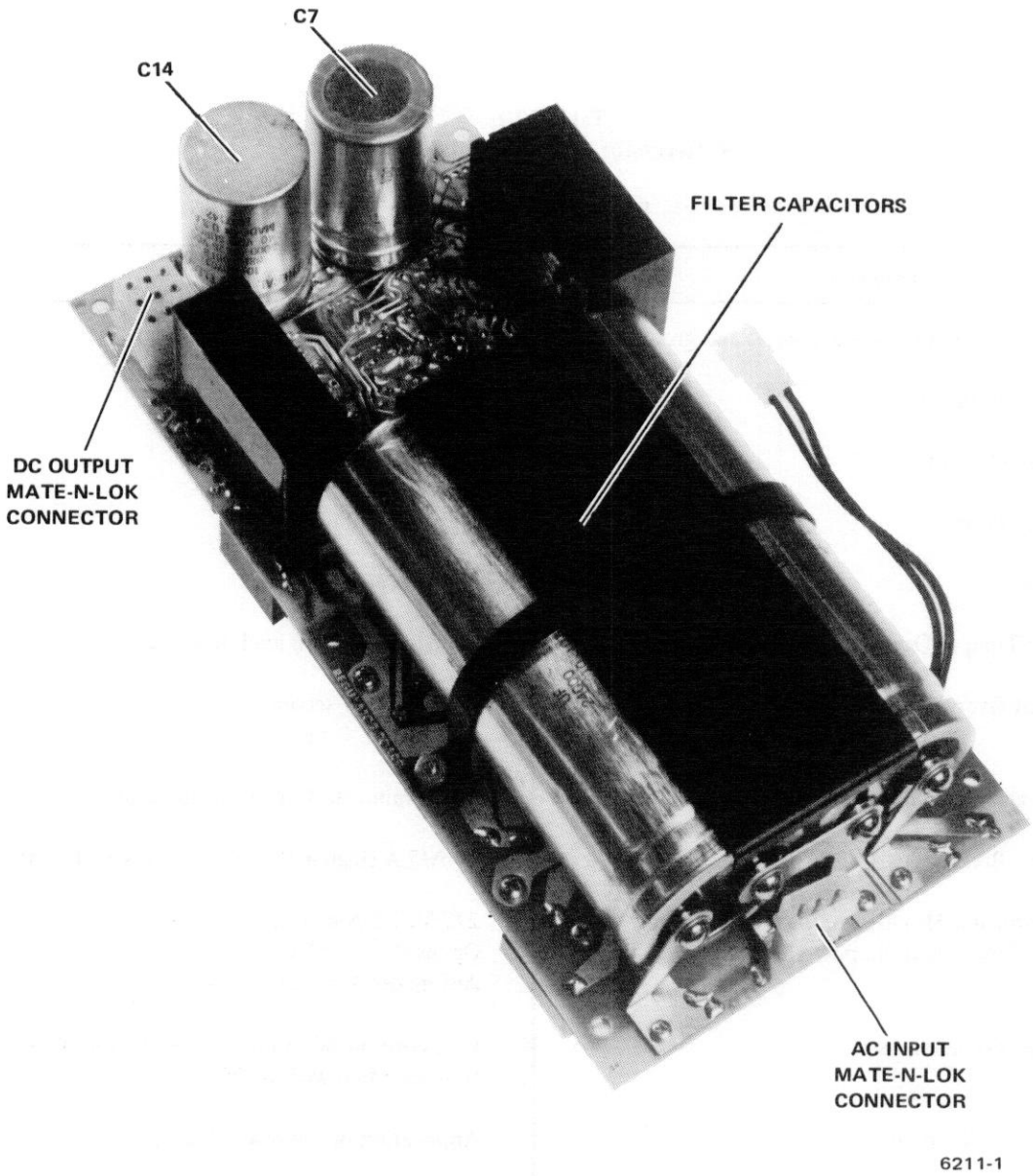


Figure 19-4 DC Regulator, Bottom View

The printed circuit board measures approximately 10 in. long by 5 in. wide with about half of the top surface devoted to the heat sink. The power transistors and power rectifiers are bolted to two shelves on the sides of the heat sink and make contact with the circuit board directly underneath via solder and screw connections. The heat sink is hard anodized for electrical insulation.

The other half of the top surface is devoted to interconnecting and mounting the balance of the circuit components. Three output voltage adjustment potentiometers (+5 V, +15 V and -15 V) are accessible on the top surface of the board.

Table 19-1
DC Regulator 5409728 Specifications

Input Specifications

Parameter	Specification
Input Voltage (1 phase, 2 wires and ground)*	95–135/190–270 V
Input Frequency	47–63 Hz
Input Current	5/2.5 A rms
Input Power	325 W at full load
Inrush	80/40 A peak, 1 cycle
Rise Time of Output Voltages	30 ms max. at full load, low line
Input Overvoltage Transient	180/360 V, 1 second 360/720 V, 1 ms
Storage After Line Failure	25 ms min., starting at low line, full load
Input Breaker (part of BC05 line set)	10 A/5 A single-pole, manually reset, thermal
Thermostat Mounted on heat sink (opens transformer and fan power)	277 V, 7.2 A contacts Opens 98°–105° C Automatically resets 56°–69° C
Input Connections	Line cord on BC05 line set, length and plug type specified with BC05
Turn-On/Turn-Off	Application or removal of power
Hipot (input to chassis and output)	2.1 kV/dc, 60 seconds

*Input voltage selection, 115 or 230 V, is made by specifying the appropriate line set, DEC Model BC05T or BC05U. All specifications are with respect to the BC05 input.

Continued

Table 19-1 (Cont)
DC Regulator 5409728 Specifications

Output Specifications

Parameter	Specification
+15 V	
Load Range	
Static	0–1 A
Dynamic	0–1 A
Max. Bypass Capacitance in load for 30 ms turn-on	500 mF
Overvoltage protection	None
Current limit at 25° C	1.3 A to 1.7 A (-6.2 mA/° C)
Backup Fuse	15 A (also used for +5 V)
Adjustment	±5% min.
Regulation (All causes including line, load, ripple, noise, drift, ambient temperature)	±5%
+5 V	
Load Range	
Static	0–15 A
Dynamic #1	±5 A (within 0–17 A load range)
Dynamic #2	No load – full load
Max. Bypass Capacitance in load for 30-ms turn-on	2000 μF
Overvoltage Crowbar (blows fuse)	5.7–6.8 V actuate (7 V abs. max. output)
Current Limit at 25° C	24–29.4 A (-0.1 A/° C)
Backup Fuse (series with raw dc)	15 A
Adjustment Range	±5% min.
Regulation	
Line	±0.5%
Static Load	3%
Dynamic Load #1	±2%
Dynamic Load #2	±10%
Ripple and Noise	4% peak-to-peak
1000 Hour Drift	±0.25%
Temperature (0–60°)	±1%

Table 19-1 (Cont)
DC Regulator 5409728 Specifications

Output Specifications

Parameter	Specification
-15 V	
Load Range	
Static	0–7 A
Dynamic #1	ΔI = 5 A (0.5 A/μs)
Dynamic #2	No load – full load (0.5 A/μs)
Max. Bypass Capacitance in load for 30-ms turn-on	1000 μF
Overvoltage Crowbar (blows fuse)	17.4–20.5 V (22 V abs. max. output)
Current Limit at 25° C	10–13.3 A (-0.03 A/° C)
Backup Fuse (series with raw dc)	5 A
Adjustment Range	±5% min.
Regulation	
Line and Static Load	±1%
Dynamic Load #1	±2.5%
Dynamic Load #2	±3%
Ripple and Noise	3% peak-to-peak
1000 Hour Drift	±0.25%
Temperature (0–60° C)	±1%
BUS DC LO L and BUS AC LO L	
Static Performance at Full Load (for 230 V connection, double voltages below)	
BUS DC LO L goes to high	74–80 Vac line voltage
BUS AC LO L goes to high	8–11 V higher
BUS AC LO L drops to low	80–86 Vac line voltage
BUS DC LO L drops to low	7–10 V lower
Hysteresis (contained in above specifications)	3–4 Vac
Output voltages still good	70 Vac line voltage

Table 19-1 (Cont)
DC Regulator 5409728 Specifications

Output Specifications

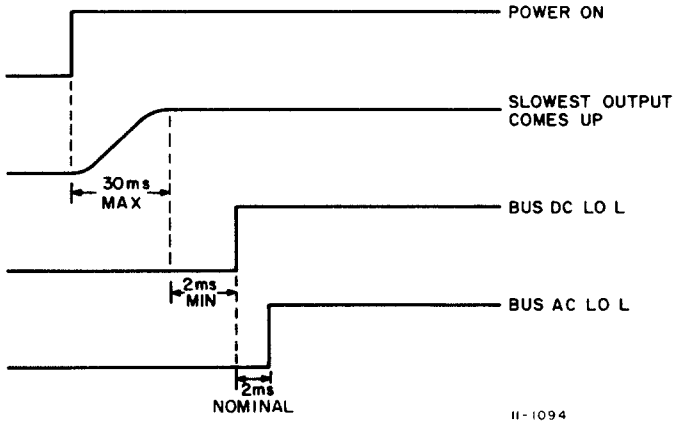
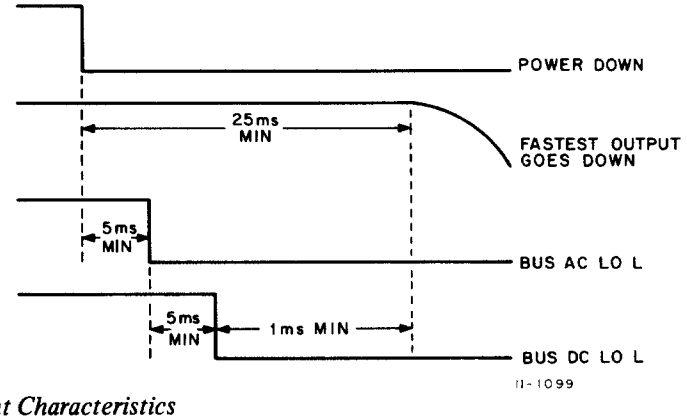
Parameter	Specification
BUS DC LO L and BUS AC LO L (Cont)	
Dynamic Performance	
Worst case on power-up is high line, full load.	
Worst case on power-down is low line, full load.	
Output Characteristics	
Open Collector	50 mA sinking capability +0.4 V max. offset
Pull-Up Voltage on Unibus	5 V nominal, 180 Ω impedance
Rise and Fall Times	1 μs max. Outputs shall remain in 0 state subsequent to power failure until power is restored despite Unibus pulling voltages remaining.

Table 19-1 (Cont)
DC Regulator 5409728 Specifications

Mechanical and Environmental Specifications

Parameter	Specification
Weight	7 lb approx. 18 lb approx.
Dimensions	10.50 in. length 5.19 in. width 3.25 in. height
Minimum Cooling Requirements	375 ft^3/min through heat sink 250 ft^3/min over caps, chokes, and transformer
Rated Heat Sink Temperature	95° C max.
Shock, Non-Operating	40 G (duration 30 ms) 1/2 sine in each of six orientations
Vibration, Non-Operating	1.89 G rms average, 8 G peak; varying from 10 to 50 Hz, 8 dB/octave roll-off 50–200 Hz; each of six directions
Ambient Temperature	0 to +60° C operating -40 to +71° C storage
Relative Humidity	95% max. (without condensation)
Altitude	10K ft

Two small Pico (TM) fuses are soldered to split lug terminals on the fan end of the PC board. These fast-acting fuses blow only when some component is defective or when the +5 V or -V is too high. The two input filter capacitors are held to the underside of the board by a bracket and are connected to the circuit via jumper tabs on the fan end.

The +5 V and -15 V output filter capacitors and inductors are mounted on the bottom surface of the board. The capacitors (C7 and C14) are attached with screws that are threaded into the capacitor terminals. The inductors (L1 and L2) are attached with integral terminal studs that pass through the board and are secured by Kep nuts.

19.2.1.2 +5 V Regulator – The H744 +5 V Regulator (Figures 19-5 and 19-6) consists of a printed circuit board, heat sink, discrete electronic components, input/output connector, and attaching hardware mounted on a sheet metal bracket.

The main structural member is a U-shaped sheet metal bracket that measures approximately 8 in. high X 5-1/4 in. wide X 2-3/4 in. deep. The heat sink is mounted in the open top of the bracket with its cooling fins facing outward and component mounting surface facing inward. It is held by two screws on each side that pass through holes in the bracket and are threaded into holes in the heat sink.

The printed circuit board is mounted with its component side facing inward on the rear of the bracket. It is mounted on two corner lugs on the lower edge of the bracket by two screws that pass through the board and are threaded into inserts in the lugs. The top of the board is attached to the rear side of the heat sink by the same hardware that is used to attach the transistor (Q2) and diodes (D4 and D5) to the top side of the heat sink. The large input filter capacitor (C1) is retained in an L-shaped holder that is attached to the bottom and left side of the bracket with two screws. The capacitor is electrically connected by two straps that are secured to the capacitor terminals with screws and are soldered to the printed circuit board. Output capacitors (C8 and C9) are mechanically and electrically connected to the printed circuit board with screws. The output inductor (L1) is mechanically and electrically connected to the printed circuit board with integral terminal studs that pass through the board and are secured by Kep nuts.

The input/output Mate-N-Lok connector is attached to the bottom right side of the board and is accessible through a hole in the side of the bracket.

A small notch in the bottom of the bracket provides access to the voltage adjustment potentiometer.

A clear plastic cover is mounted on four mounting lugs on the front of the bracket. It is held by four standoffs that have male threads on one end to attach the cover and female threads on the other end by which the regulator is mounted to the power supply chassis.

19.2.2 Line Set

The line set consists of a BC05T (115 V) or BC05U (230 V) ac power cord installed in and wired to an ac input box (drawing C-UA-BC05T-0-0 or C-UA-BC05U-0-0). The box is a U-shaped sheet metal bracket with a slide-on cover that is locked in place with one screw (Figures 19-7 and 19-8). The box contains a circuit breaker, printed circuit board, RFI dual-disc ceramic capacitor, and a 6-socket Mate-N-Lok connector. The circuit breaker is mounted on one end of the box so that the reset button is accessible when the line set is installed in the computer. The printed circuit board is mounted on the circuit breaker terminals with two screws to provide the electrical interconnection for the circuit breaker. The board is used to mount and interconnect the RFI capacitor, Mate-N-Lok connector, and Faston tab connectors for the ac power cord. The phase (black) and neutral (white) wires of the ac power cord are connected directly to the Faston tabs on the printed circuit board. The ground (green) wire of the ac power cord is connected to a dual Faston tab on the bracket and then to the Faston tab on the printed circuit board.

The 115 V and 230 V models differ in two respects: breaker current rating (10 A for 115 V and 5 A for 230 V) and the layout of the printed circuit jumpers for connection to the transformers.

(TM) Pico is a trademark of Littlefuse Electrical Supply.

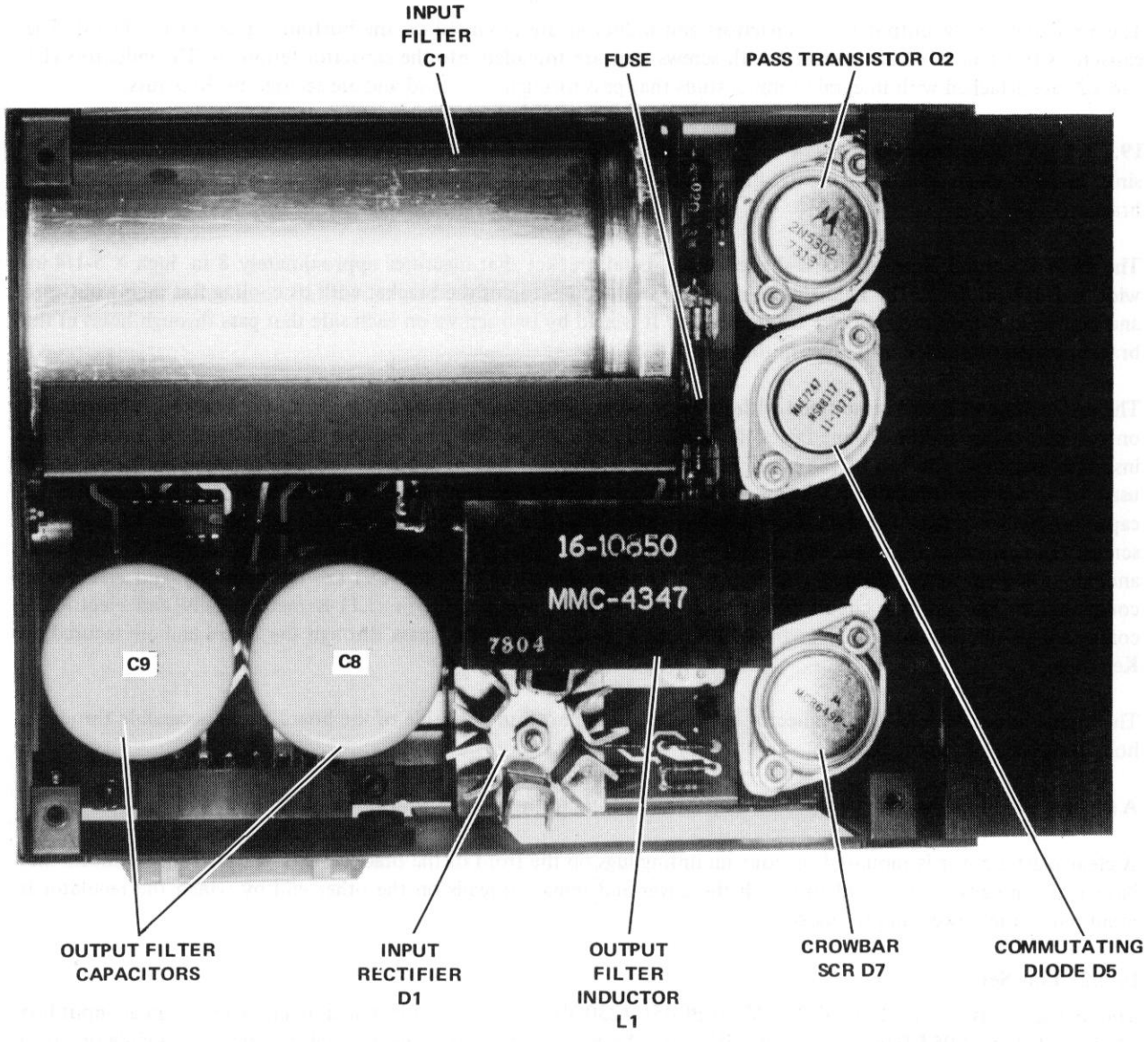


Figure 19-5 +5 V Regulator, Side View

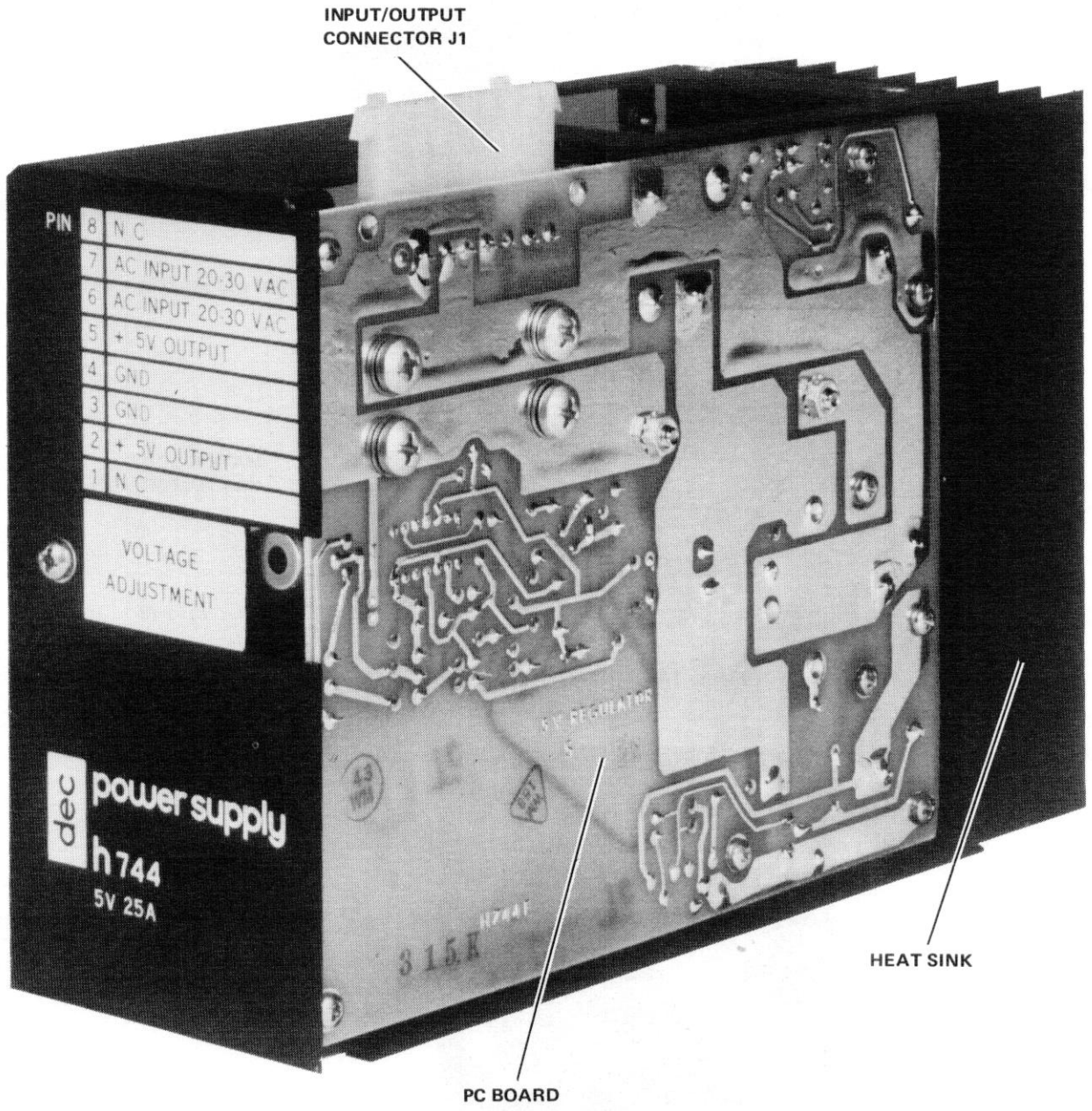


Figure 19-6 +5 V Regulator, 3/4 Bottom View

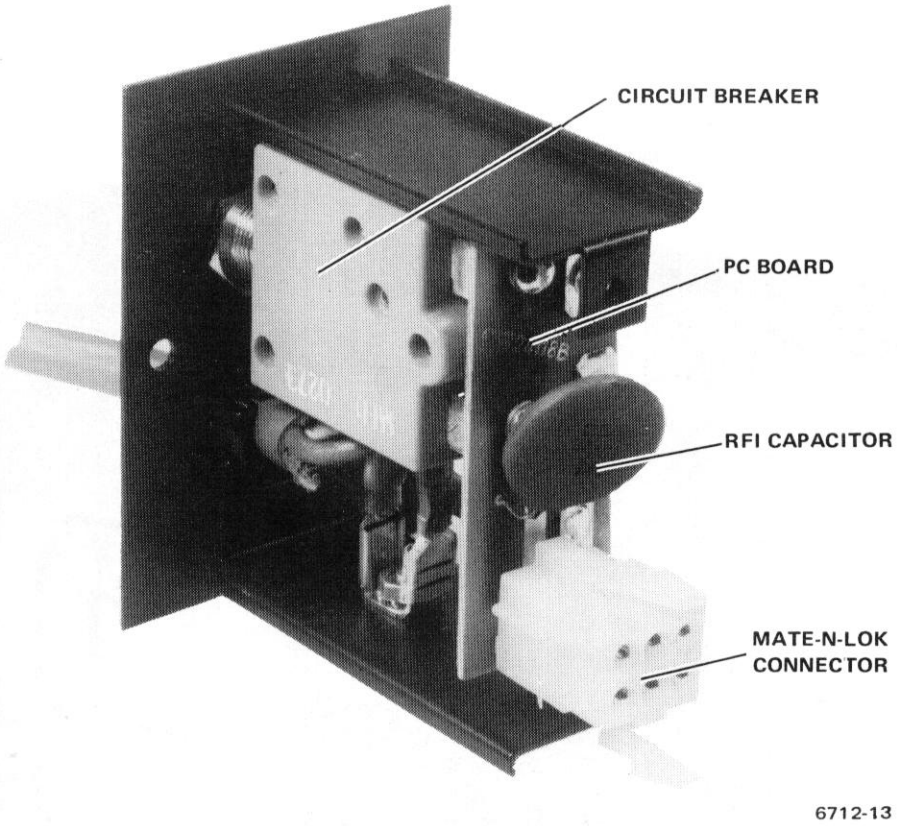


Figure 19-7 BC05T Line Set, Cover Removed

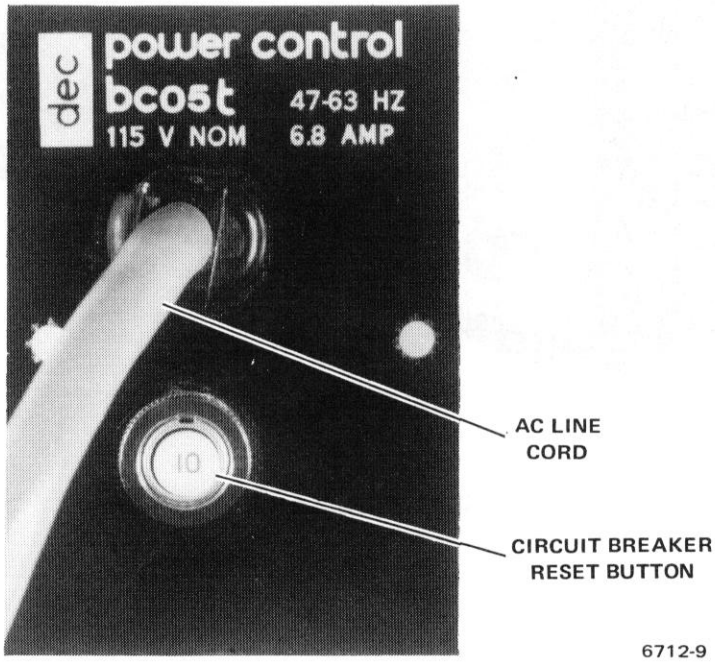


Figure 19-8 BC05T Line Set, Rear View

19.2.3 Wiring Harnesses

Two mechanical features concerning the wiring harnesses are worth mentioning. One is that terminal block TB1 is considered part of the power supply harness (drawing E-IA-7009207-0-0). It is a Cinch #8-540 and contains eight pairs of screw type terminals.

The other feature is that the power distribution board is part of the power to distribution board harness (drawing E-IA-7009208-0-0). It is a printed circuit board and the harness wires are soldered to eyelets on the board. The signals on these wires are connected to five identical 9-pin Mate-N-Lok connectors on the board via the etched circuit.

19.3 SYSTEM FUNCTIONAL DESCRIPTION

A functional block diagram of the power system is shown in Figure 19-9. Assume that the line cord is plugged in and the console switch is OFF. Line voltage is applied to the primary of transformer T3 and produces 28 Vac in the secondary of T3, which is connected to the diode board (PS3). The diode board rectifies the secondary output of T3 to energize the coil of relay K1. The +28 V from PS3 must pass through relay coil K1, PS1 regulator, thermostat, and the console switch to ground to complete the circuit. If the console switch is OFF or the thermostat is open (overtemperature condition), relay K1 cannot be energized. This prevents ac line voltage from being applied to transformers T1 and T2 and all three fans.

When the console switch is placed in the POWER position, the relay coil circuit is completed and the relay is energized. Two sets of normally opened relay contacts now close and ac line voltage is applied to all three fans and the primaries of transformers T1 and T2. The 28 Vac secondary voltage from T1 is applied to the rectifier circuit in the PS1 regulator and the 28 Vac secondary voltage from T2 is applied to the rectifier circuit in the PS2 regulator. The outputs of the regulators are sent to the power distribution board and on to the backplane.

The power supply harness contains two Mate-N-Lok connectors that allow connection to the optional cabinet mounted power control unit. This device allows all units in a single or multi-cabinet system to be turned on using the computer console switch. The power control unit automatically removes ac line power if an overload or overtemperature condition occurs in a cabinet.

A detailed power system interconnection diagram is shown in Figure 19-10. All connector and component pins are identified to allow detailed circuit tracing.

19.4 SYSTEM CIRCUIT DESCRIPTION

19.4.1 Introduction

This paragraph provides circuit descriptions of the 115 V and 230 V line sets, power distribution board, dc regulator, and +5 V regulator.

19.4.2 Line Set

The 115 V and 230 V line sets differ only in the circuit breaker current rating and printed circuit board jumper configuration. For 115 Vac power, the jumpers connect both primaries of transformers T1, T2, and T3 to 115 Vac in parallel (Figure 19-11). For 230 Vac power, the jumpers connect both primaries of each transformer (T1, T2, and T3) to 230 Vac in series (Figure 19-12).

19.4.3 Power Distribution Board

The circuit schematic for the power distribution board is shown in Figure 19-13. The outputs of the dc regulator (PS1) and +5 V regulator (PS2) are sent via the power distribution harness to the board. The harness wires are soldered to eyelets on the board. The signals on these wires are distributed via the etch to the five 9-pin Mate-N-Lok connectors (J1–J5) on the board as shown in Table 19-2.

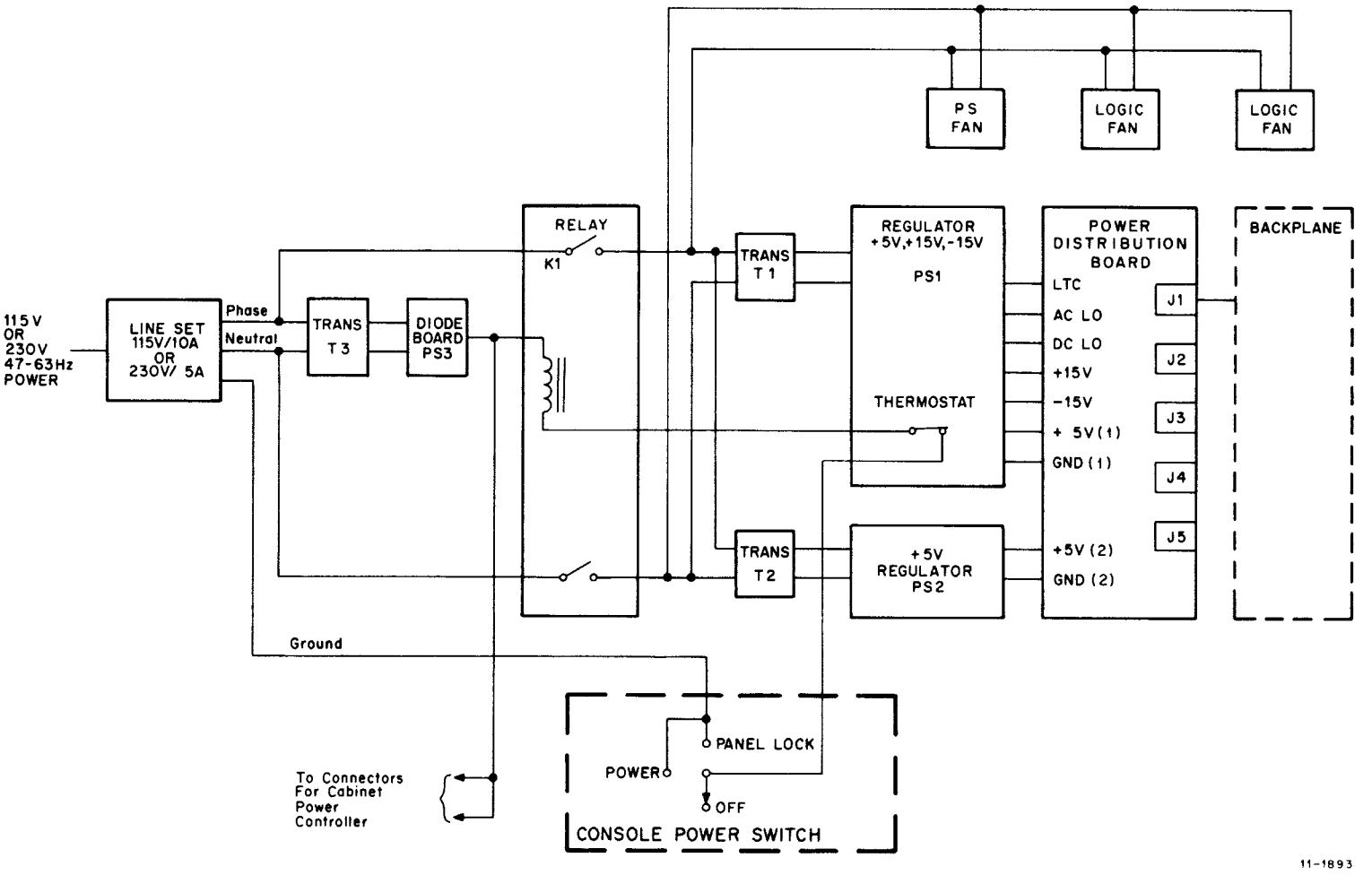


Figure 19-9 Power System Functional Block Diagram

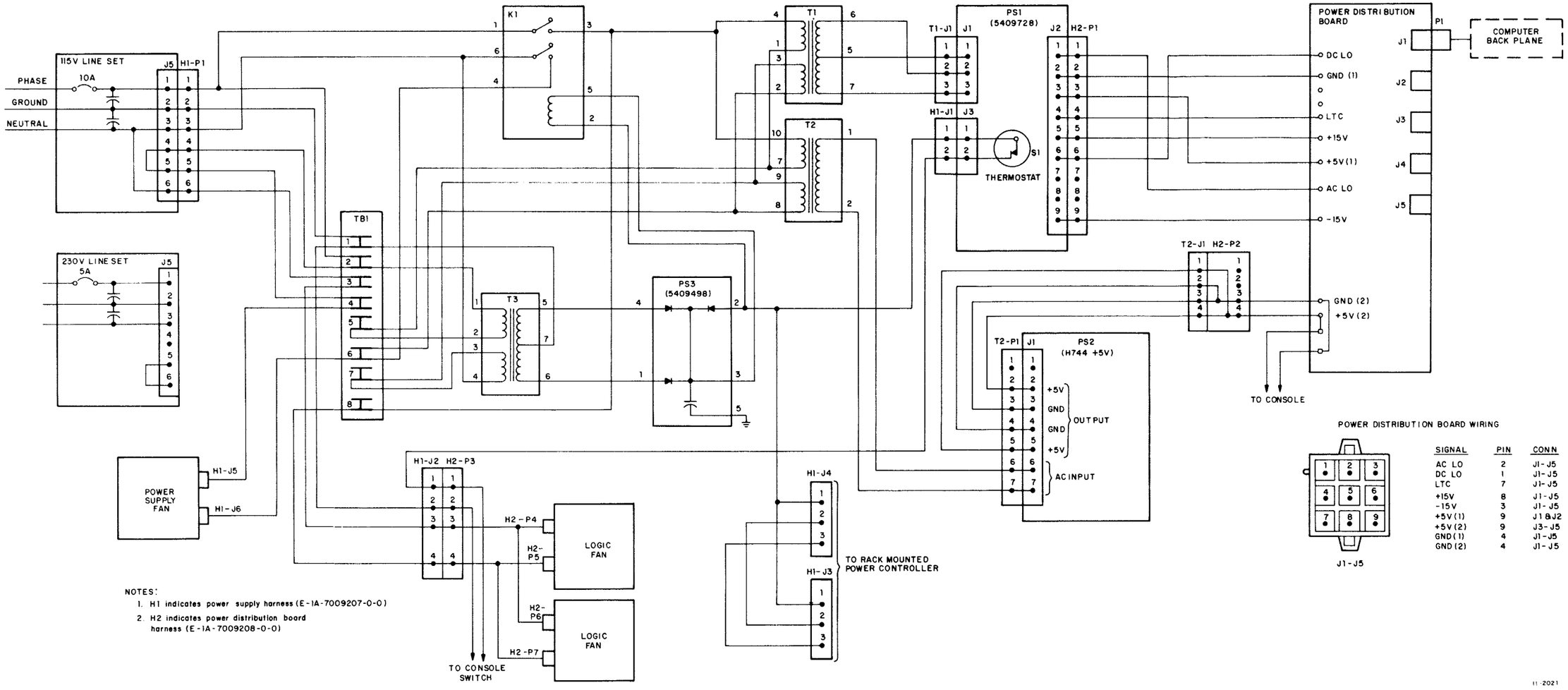


Figure 19-10 Power System Interconnection Diagram

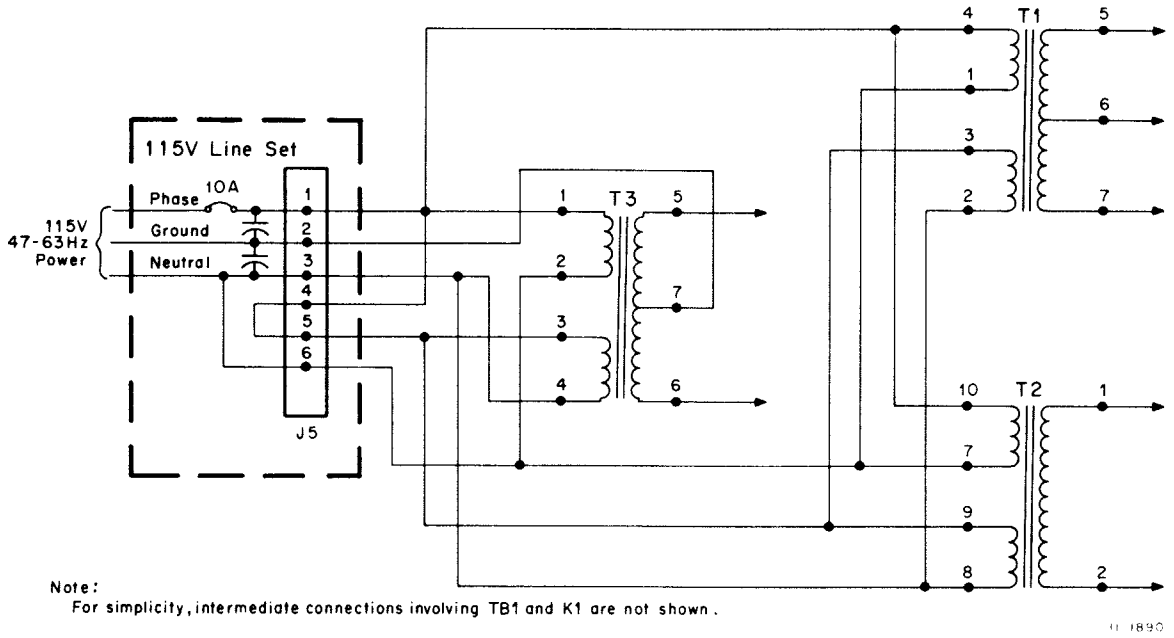


Figure 19-11 Power Applications Using 115 V Line Set

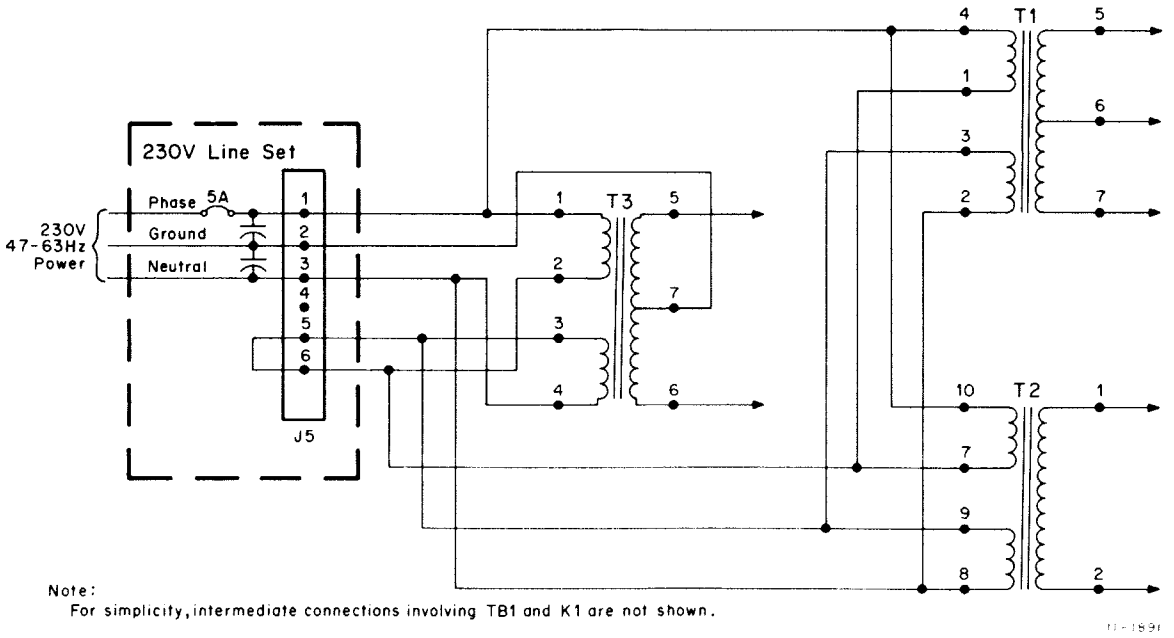


Figure 19-12 Power Application Using 230 V Line Set

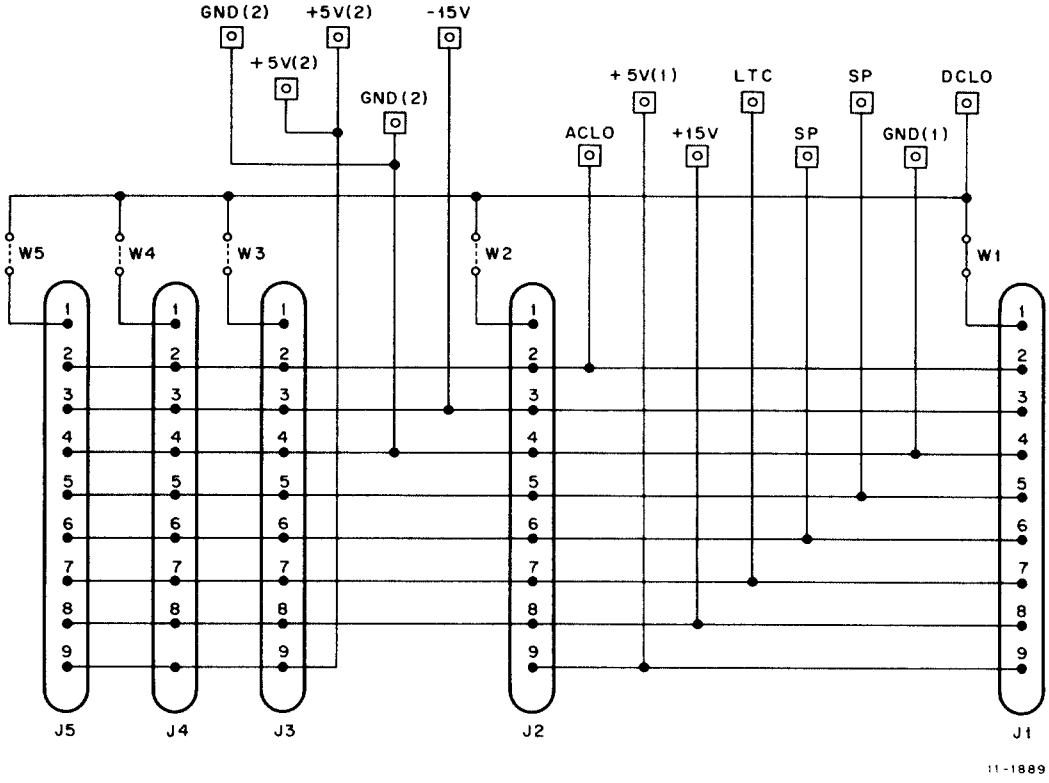


Figure 19-13 Power Distribtuion Board Circuit Schematic

Table 19-2
Power Distribution Board Signals

Source	Signal	Destination
H744 5 V Regulator	+5 V (2)	J3, J4, and J5 pin 9
	GND (2)	J1–J5 pin 4**
5409728 dc Regulator	DC LO	J1–J5 pin 1*
	AC LO	J1–J5 pin 2
	LTC	J1–J5 pin 7
	+5 V (1)	J1 and J2 pin 9
	+15 V	J1–J5 pin 8
	-15 V	J1–J5 pin 3
	GND (1)	J1–J5 pin 4**

Notes: *Connected to each Mate-N-Lok via a jumper.
**Electrically connected on the board. Pins 5 and 6 on J1–J5 are spares.

CAUTION

Output +5 V (1) is generated by the 5409728 regulator and is available on connectors J1 and J2. Output +5 V (2) is generated by the H744 Regulator and is available on connectors J3–J5. These supplies are separate and should not be connected together.

The current ratings for the power supply outputs are shown below. The ratings listed are maximum; that is, for a particular output, the sum of the loads on the connectors used must not exceed the specified value.

5409728 dc regulator

+5 V (1) on connectors J1 and J2 is 20 A total
+15V on connectors J1–J5 is 1 A total
-15 V on connectors J1–J5 is 8 A total

H744 Regulator

+5 V (2) on connectors J3, J4, and J5 is 20 A total

Parallel connections of +5 V (2) and GND (2), using Faston tabs on the power distribution board, are provided to connect these outputs to the computer console printed circuit board.

The power distribution board contains a DC LO jumper for each connector (J1–J5). Only one DC LO connection is required per mounting box. In the basic computer, jumper W1 is installed to bring the DC LO signal to the backplane because the processor power harness connects the backplane to the power distribution board at connector J1.

A jumper for each connector is provided because it is possible to mount a backplane in any position and connect it to any power distribution board connector.

The requirement for only one installed DC LO jumper per box is emphasized in the following special case.

Assume that a PDP-11/05 mounting box is to be used as an expander box with a DB11-A Bus Repeater installed along with other options. Unlike previous expansion boxes, the PDP-11/05 box allows the DB11-A to be installed in any position. When connected to the appropriate distribution board connector, the associated DC LO jumper is installed. All other DC LO jumpers must be open to prevent latching up of the DC LO circuit by looping through the power harness if more than one jumper is installed.

Options for the basic computer include a pre-wired backplane and specific power harness to connect the backplane to the power distribution board (Table 19-3).

Table 19-3
Option Power Harnesses

Option	Power Harness
MF11-L	70-09206
DD11-B	70-09099
DD11-A	70-09205*

*Not shipped with computer. Harness must be ordered separately to install customer's DD11-A.

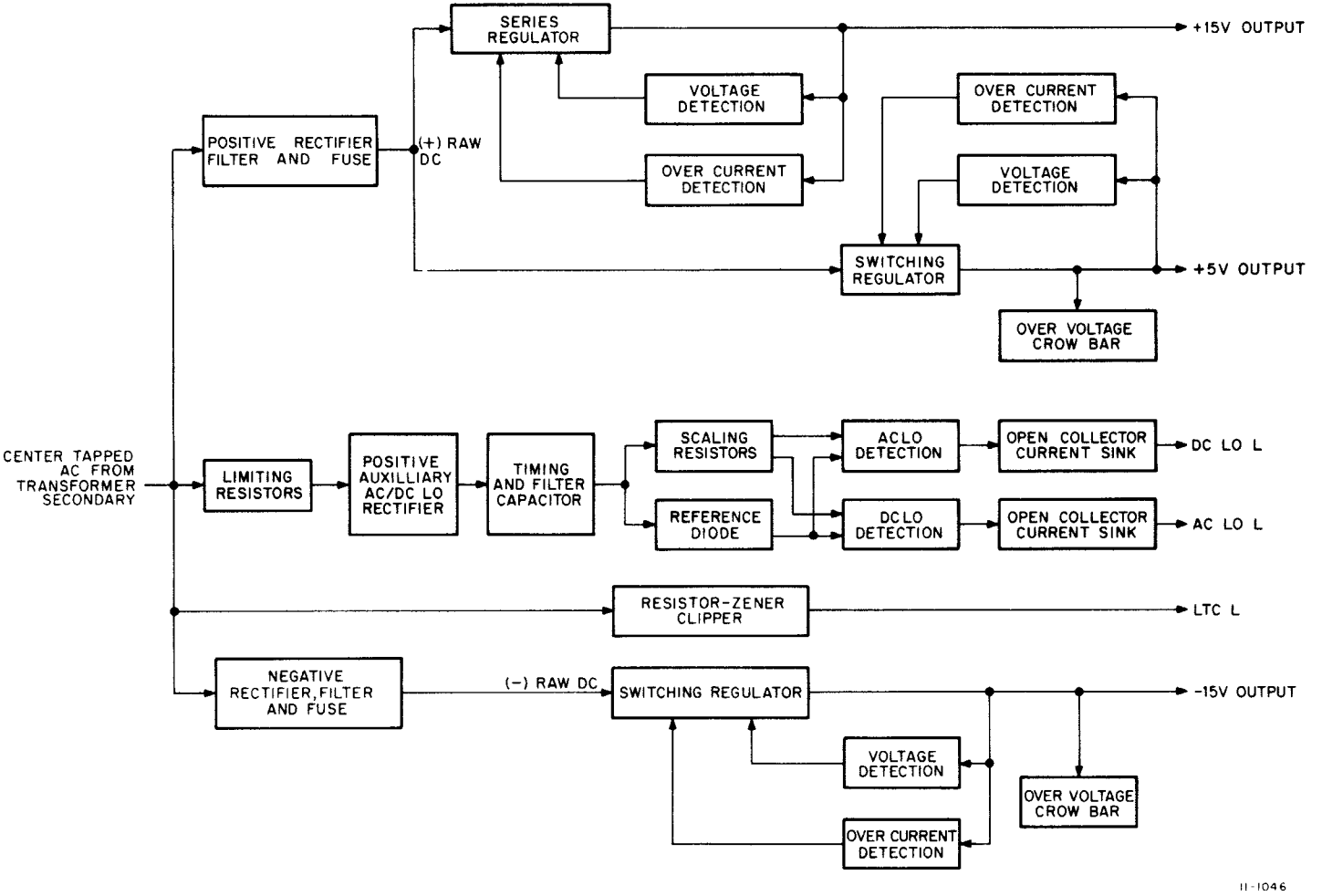


Figure 19-14 DC Regulator Block Diagram

The DD11-A and DD11-B are pre-wired backplanes used to mount up to four small peripheral interfaces (equivalent to four quad boards). The DD11-B is a later version of the DD11-A that uses Faston tabs on the wire-wrap pin side to connect with the power harness. The DD11-A uses a power harness that contains a cable connector module which plugs into the connector side of the backplane. The DD11-A is not shipped with the computer; rather, the later DD11-B version is used. If the customer has a DD11-A and wants to install it in the computer, he must order power harness 70-09205.

The KD11-B Processor requires 8.0 A at +5 V and 1 A at -15 V. The power requirements for the MF11-L Memory are listed below.

MF11-L Capacity	Current at +5 V	Current at -15 V
8K	3.4 A	6.0 A
16K	4.9 A	6.5 A
24K	6.4 A	7.0 A

19.4.4 DC Regulator (PS1)

19.4.4.1 Functional Operation – A block diagram of the dc regulator is shown in Figure 19-14. The center tapped output of the power transformer is applied to positive and negative rectifier and filter circuits. The rectifier circuits produce +39 V and -29 V nominal raw dc voltages, which are unregulated but well filtered by the input storage capacitors.

The +39 V is used by an efficient switching regulator circuit to produce the +5 V output. Provisions for overcurrent detection are incorporated in the regulator circuit so that excess current is limited when there is a malfunction in the load. The +5 V output is also protected against overvoltage by a crowbar circuit which limits the output to an absolute maximum of 7 V; at approximately 6 V, the crowbar circuit blows fuse F1 in the output circuit of the rectifier.

The +15 V output is produced by a series regulator circuit. It has no overvoltage protection circuit. Fuse F1 is used for protection in case of a malfunction in the +15 V regulator.

The -39 V is used by the -15 V circuit, which is similar in operation to the +5 V regulator circuit. The -15 V crowbar circuit limits the output to an absolute maximum of -22 V. At approximately -19 V, the crowbar circuit blows fuse F2 in the output circuit of the rectifier.

The real-time clock synchronizing signal (LTC L) is generated by a simple Zener clipper that is fed from the transformer secondary.

The BUS AC LO L and BUS DC LO L signals are used to warn the Unibus of imminent power failure. Circuits detect the transformer secondary voltage and generate two timed TTL-compatible open-collector signals that are used for power fail functions by devices on the Unibus.

19.4.4.2 Generation of Raw DC Voltages – As stated in the previous paragraph, the centertapped transformer secondary voltage is rectified and filtered prior to being fed to the three dc regulators.

The circuitry is shown in Figure 19-15. Bridge rectifier D14 is mounted on the heat sink and input capacitors C1 and C2 are mounted on the bottom of the regulator module. These capacitors filter the input dc and are large enough to provide power storage for at least 25 ms when the input power is shut off or fails.

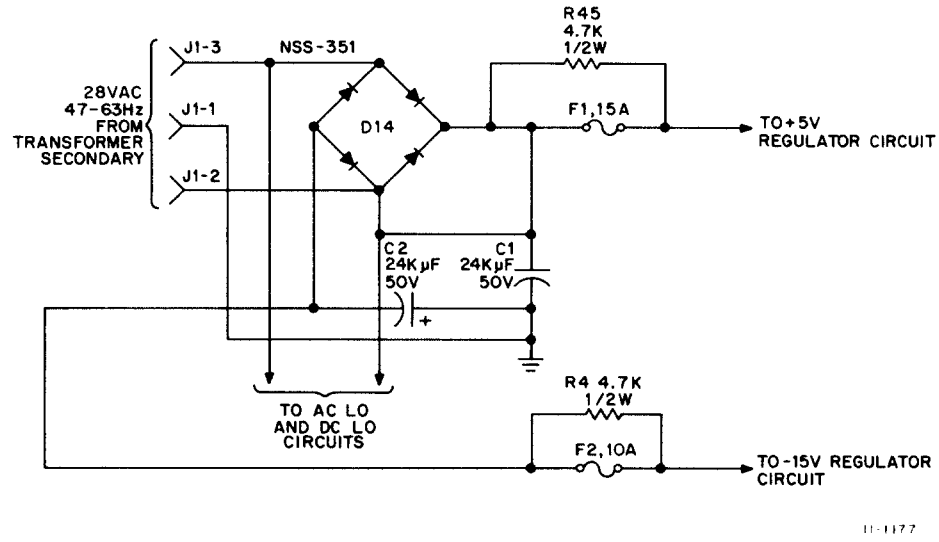


Figure 19-15 Rectifier and LTC Circuits

Two fuses are used to protect the regulator and load during faults. A 15 A fuse protects both the +5 V and +15 V outputs and a 5 A fuse protects the -15 V output. Normally, the fuses do not blow when a regulator output is shorted because the three outputs are electrically overcurrent protected. However, the appropriate fuse does blow in case of +5 V or -15 V overvoltage crowbar or in case of failure in one of the overcurrent circuits.

The resistor across each fuse provides a slow (100 – 150 seconds) discharge of C1 or C2 when the power is turned off after a fuse has blown. The capacitors are placed ahead of the fuse to limit the energy in any fault and thus better protect the outputs.

19.4.4.3 LTC L Circuit – The LTC L real-time clock synchronizing signal (Figure 19-15) is generated by a Zener clipper circuit. The output waveform is a clipped sine wave at line frequency. For the positive half of the output sine wave, D13 clips at about +3.9 V and for the negative half D13 clips at its forward voltage of -0.7 V.

19.4.4.4 BUS AC LO L and BUS DC LO L Circuits – The circuitry shown in Figure 19-16 is used to generate the timed Unibus power status signals that are used for power fail function.

The transformer secondary voltage is rectified by D1 and D2 and filtered by C9 and R1, R14. Circuit parameters are chosen so that the voltage across C9 rises slower than the three regulated output voltages on powerup and decays faster than the three regulated output voltages on powerdown.

Two differential amplifier circuits are used to detect power status: Q17, Q18 generates BUS DC LO L; and Q15, Q16 generates BUS AC LO L. Both differential amplifiers share a common reference Zener diode D3, which is fed approximately 1 mA by R3.

As C9 charges subsequent to powerup, first Q17, Q18, and then Q15, Q16 change state; the reverse is true during powerdown. When C9 starts to charge, Q17 and Q16 are on and Q15 and Q18 are not conducting. As C9 charges further, Q18 starts to conduct into R7 and raises the voltage on the cathode of D3. This acts as positive feedback and snaps Q17 off and Q18 on more solidly. A few milliseconds later, the voltage across C9 has risen sufficiently for the same process to take place in differential amplifier Q15, Q16. The status of each differential amplifier is followed by the germanium transistor open-collector output stages Q19, Q20 for BUS DC LO L, and Q13, Q14 for BUS AC LO L. These stages clamp the Unibus at about +0.4 V until the differential amplifier circuits sequentially signal them across R11 and R12 that power is up. The outputs then rise to about +5 V as dictated by the Unibus loading and pull-up termination resistors.

The sequence is as follows:

powerup → then BUS DC LO L = 0 → then BUS AC LO L = 0
0 = high (+3 V)

powerdown → then BUS AC LO L = 1 → then BUS DC LO L = 1
1 = low (+0.4 V)

During a power-down sequence, after BUS AC LO L goes low, there is sufficient storage in capacitors C1 and C2 to maintain output voltage long enough to permit the power fail circuit to operate. The open collector stages are designed to clamp the Unibus to 0.4 V maximum, even when there is no ac input to the regulator. They are inherently biased on by R11 and R12 until the differential amplifiers signal that power is OK.

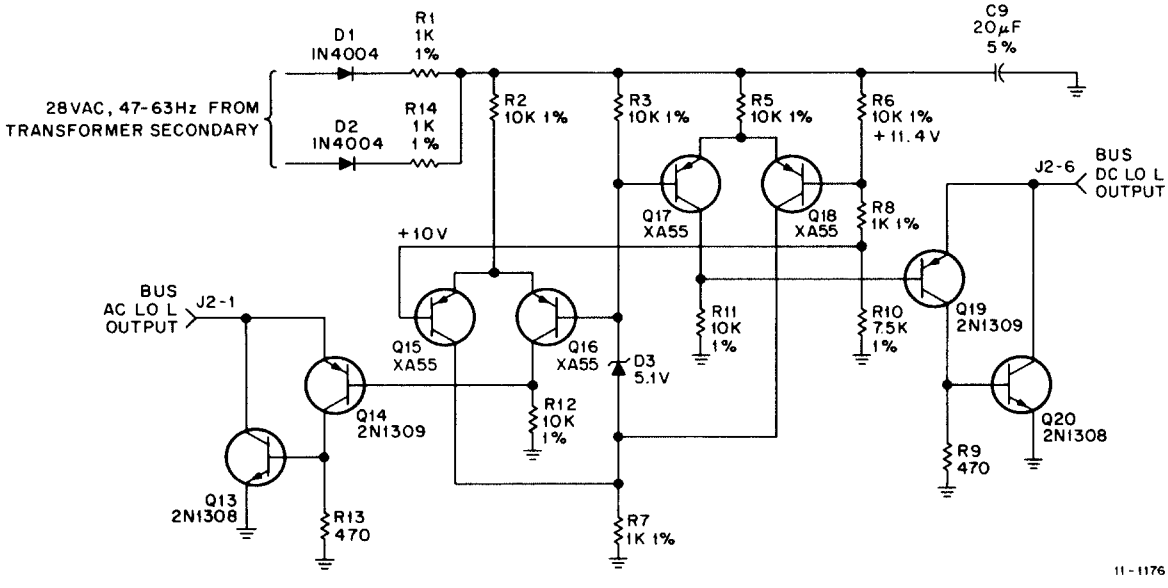


Figure 19-16 BUS AC LO and BUS DC LO Circuits

19.4.4.5 +15 V Regulator Circuit – The +15 V regulator shown in Figure 19-17 is a simple series regulator. The pass transistor Q1 is a high-gain power Darlington type and is mounted on the heat sink. Base drive current is supplied to Q1 via R38. Q3 limits the value of this current to the required value by shunting it away from the Q1 base. Voltage detector amplifier Q4 biases on Q3 and thus limits current in Q1. The +15 V output voltage is sampled on the viewing chain R34, R35, R36 and compared to the voltage across reference Zener D8, which is fed by R37. If the output tries to increase from the regulated value, the emitter of Q4 is made more negative (relatively) than its base and conduction through Q4 increases. This increases the conduction through Q3 and causes Q1 to shut down sufficiently to restore the output voltage to the regulated value. Ambient temperature compensation of the voltage detector is essentially flat since D8 has a +2 mV/° C temperature coefficient and the base emitter junction of Q4 has a -2 mV/° C temperature coefficient.

R35 is the +15 V voltage adjustment potentiometer and C18 is a high frequency stabilization capacitor. Q2 is the overload detector; when the output current reaches 1.5 A nominal, the voltage across R33 is sufficient to cause Q2 to conduct which removes base drive from Q1 and causes the regulator to current limit.

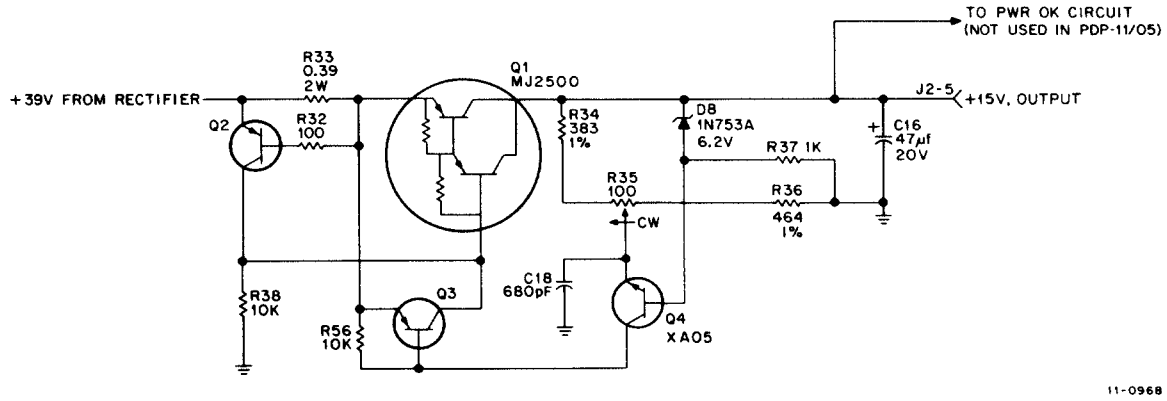


Figure 19-17 +15 V Regulator Circuit

19.4.4.6 +5 V Regulator Circuit – The +5 V regulator is similar to the +15 V regulator in that the sampled output voltage is compared to the voltage across a reference Zener by a voltage detector transistor, which, in turn, controls the drivers for the main pass transistor. An overcurrent circuit is used also. The +5 V regulator circuit is shown in Figure 19-18.

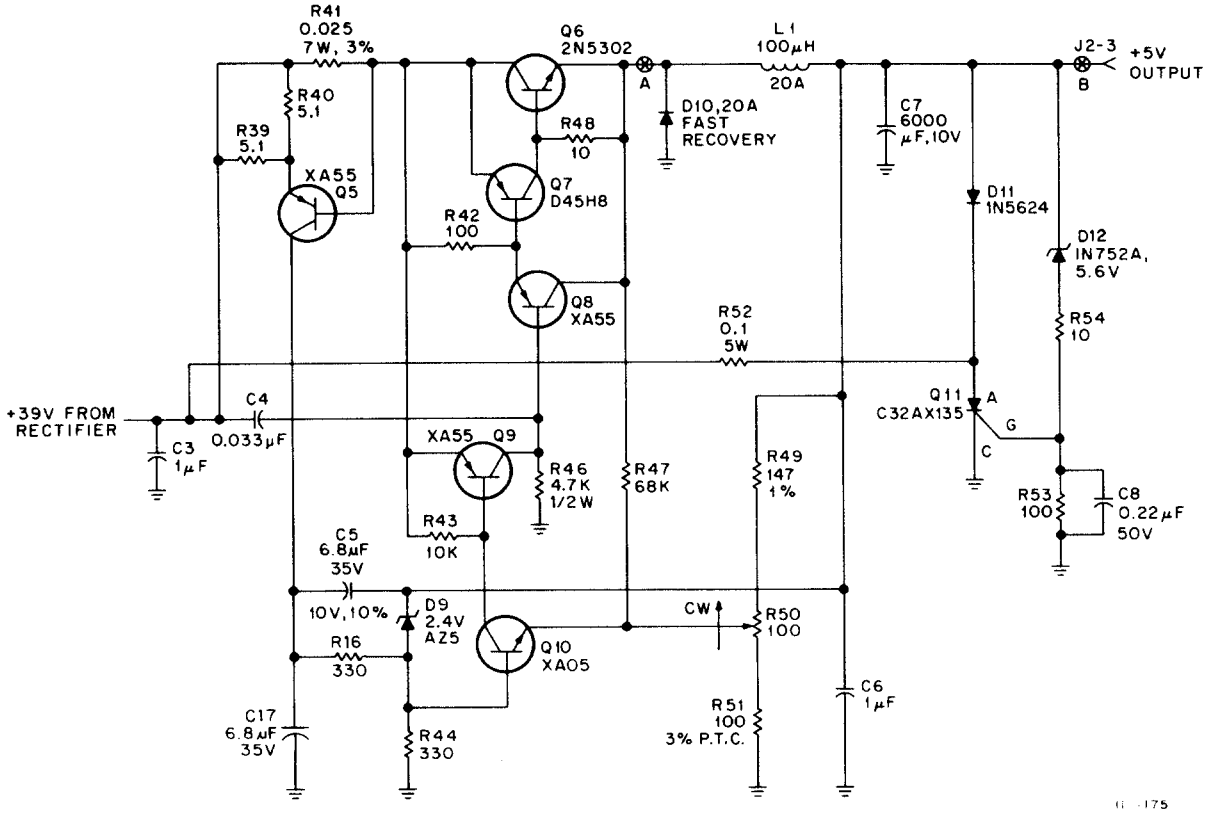


Figure 19-18 +5 V Regulator Circuit

The viewing chain consists of R49, R50, and R51. The reference Zener is D9, which is fed by R44. Q10 is the detector amplifier. The pass transistor Q6 and first stage driver Q7 are mounted on the heat sink. The predriver Q8 is turned on by R46. The current is diverted from the base of Q8 by off-driver Q9, which is controlled by Q10. The +15 V and the +5 V regulators are similar in operation; i.e., a tendency for the output voltage to rise results in more conduction through Q10 and resultant limiting of conduction through Q6.

Here the similarity ends. The +5 V regulator operates in the switching mode for increased efficiency. To get the regulator to switch, positive feedback is applied to the voltage detector input via R47. Thus, the whole regulator acts as a power Schmitt trigger and is either completely turned on or turned off, depending on whether the output voltage is too high or too low. When Q6 is on, it supplies current through filter choke L1 to the output smoothing capacitor C7 and the load. When Q6 is off, the L1 current decays through commutating diode D10, which becomes forward biased by the back emf of L1. The waveform across D10 is a 30 V nominal rectangular pulse train. The filtered output across C7 is thus +5 Vdc with about a 200 mV peak-to-peak 10 kHz nominal sawtooth of superimposed ripple. At the crest of the ripple, Q6 turns off and at the valley Q6 turns on. This switching mode of operation limits the dissipation in the circuit to the saturated forward losses of Q6 and D10 and the switching losses of Q6. The resultant high efficiency allows the use of a small heat sink and relatively few power transistors.

R50 is the voltage adjustment potentiometer. R51 is a positive temperature coefficient wire-wound resistor that compensates for the fact that the Q10 base-emitter junction and the reference diode D9 both have negative voltage temperature coefficients. Q5 current, limited by R39 and R40, detects the overcurrent signal generated across resistor R41, which is in series with the Q6 collector.

Output fault current is limited to a safe value because conduction of Q5 makes the reference voltage across D9 decrease to zero. This causes Q10 to conduct and shuts down the regulator. C5 is an averaging capacitor, which is necessary in the circuit because the current through R41 is pulsating.

High frequency bypass capacitors are used on the input and output of the regulator (C3 and C6, respectively) and C4 is used to slow down the turn-on of Q6 to allow D10 to recover from the on state without a large reverse current spike.

If a malfunction causes the output voltage to increase beyond about 6 V, Zener diode D2 conducts and fires silicon-controlled rectifier Q11. This crowbars the output voltage to a low value through D11 and blows fuse F1 in the rectifier circuit through R52.

19.4.4.7 -15 V Regulator Circuit – The -15 V regulator circuit is shown in Figure 19-19. It is essentially the complement of the +5 V regulator circuit and differs only in the following minor details.

a. The crowbar device is a Triac (Q27) instead of an SCR. No temperature compensating resistor is required because Q26 and D4 track each other, as in the +15 V regulator.

b. The detailed interconnection of the drivers and the circuit values are different.

c. The -15 V output voltage is adjusted by potentiometer R26.

19.4.5 +5 V Regulator (PS2)

19.4.5.1 Functional Operation – A functional block diagram of the +5 V regulator is shown in Figure 19-20. The 28 Vac from the secondary of transformer T2 is full wave rectified and filtered. This raw dc voltage (approximately 39 V) is used by a switching regulator circuit to produce the +5 V output. An overcurrent detection circuit is incorporated in the regulator circuit to limit excess current when there is a fault in the load. The +5 V output is also protected against overvoltage by a crowbar circuit that limits the voltage to +7 V. Before the output reaches +7 V, the crowbar circuit blows the fuse in the rectifier output. A circuit schematic of the +5 V regulator is shown in Figure 19-21 and is referenced in the subsequent paragraphs.

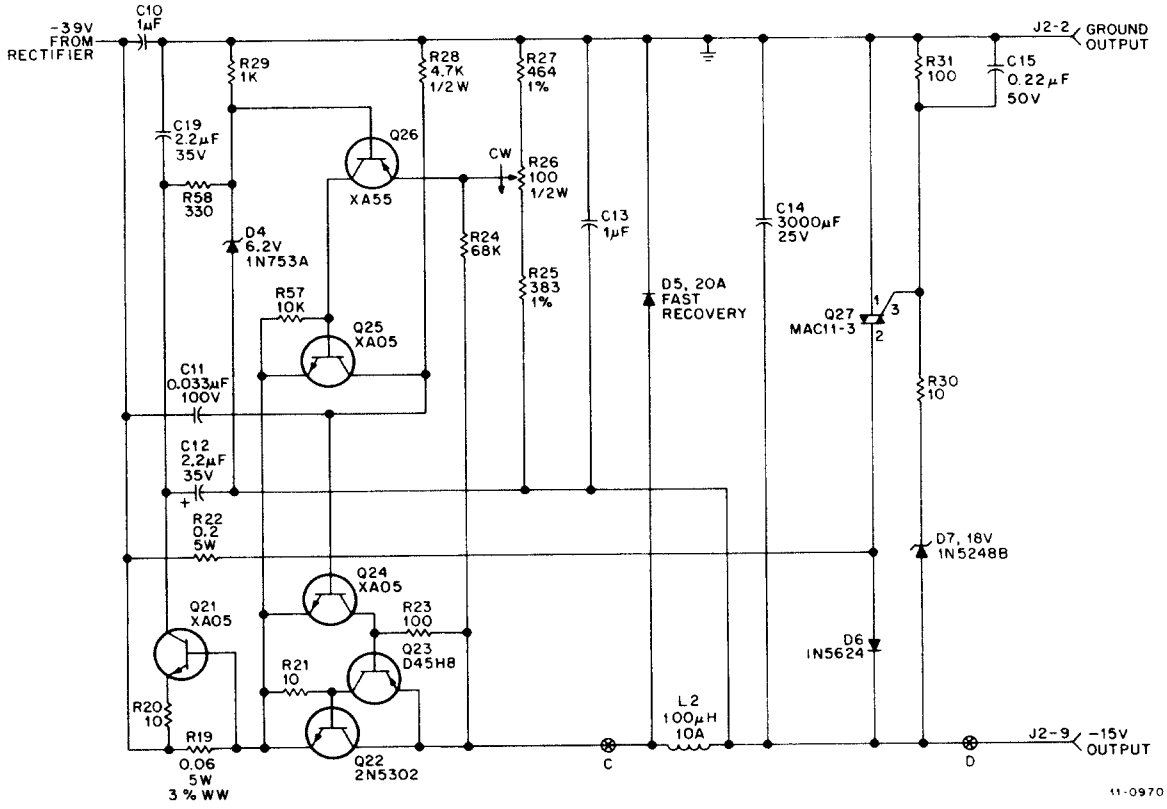


Figure 19-19 -15 V Regulator Circuit

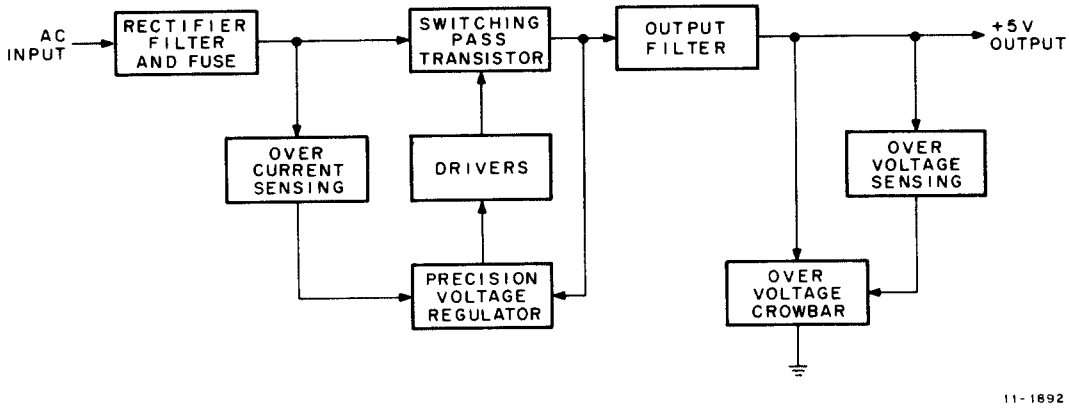


Figure 19-20 +5 V Regulator (PS2) Functional Block Diagram

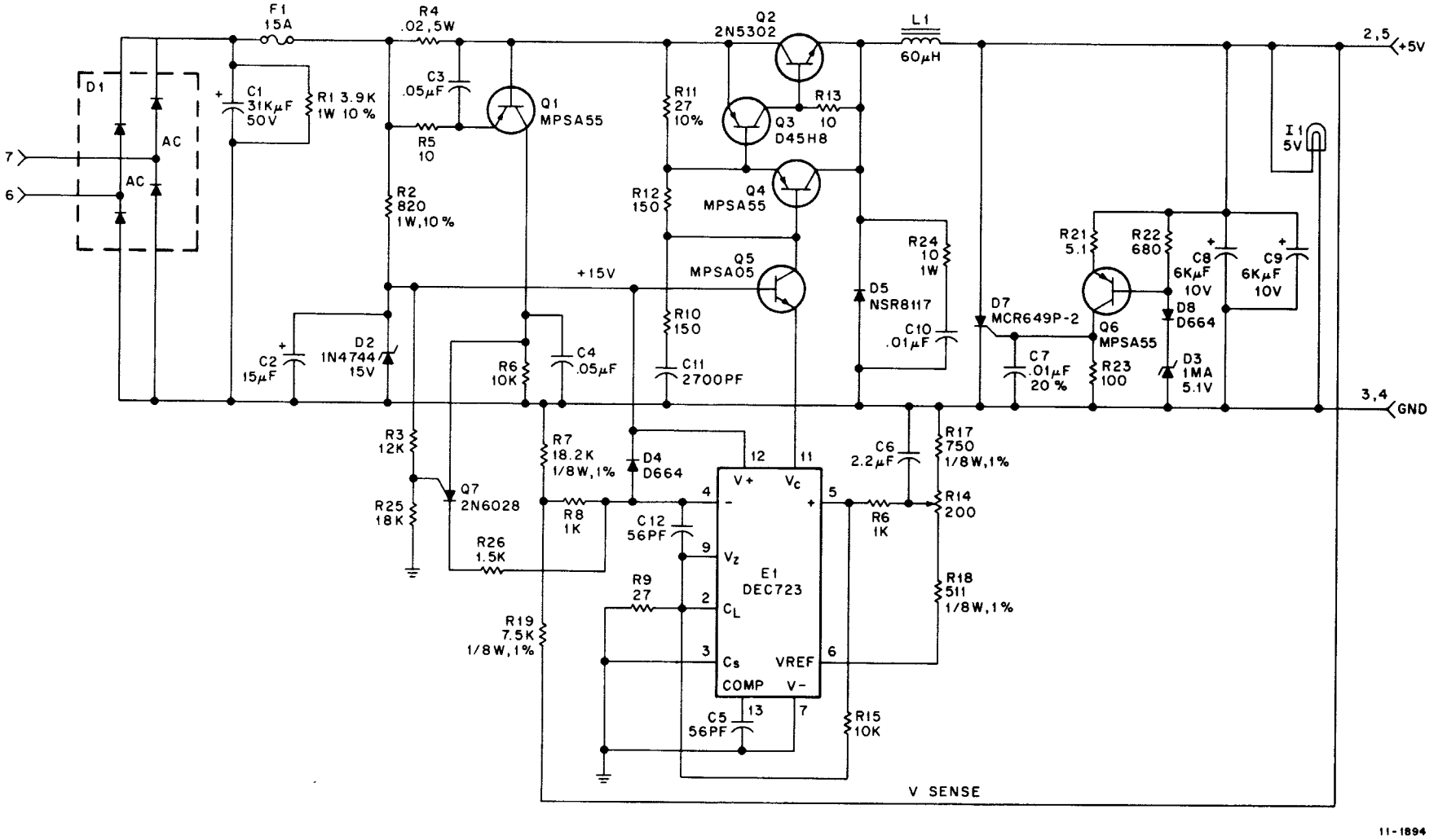


Figure 19-21 +5 V Regulator (PS2) Circuit Schematic

19.4.5.2 Generation of Raw DC Voltage – The 28 Vac from transformer T2 is applied to full wave rectifier D1 via pins 6 and 7 of connector J1. The rectifier output is approximately +39 V and is filtered by capacitor C1. Resistor R1 is a bleeder resistor and dissipates the charge on C1 during shutdown. The 15 A fuse (F1) protects the regulator and load during faults. Normally, the fuse does not blow when the regulator output is shorted because the output is protected against overcurrent operation. The fuse does blow if the crowbar circuit fires or in case of failure in the overcurrent protection circuit.

19.4.5.3 Regulator Circuit – The regulated +5 V is sampled by resistors R19 and R7. The magnitude of this voltage is compared to a precision 5 V reference voltage produced by voltage regulator E1 and voltage divider R17, R14, and R18. This regulator responds to ±0.05 V differences between the sensed output and the reference.

E1 is an integrated circuit in a 14-pin dual in-line package. A simplified equivalent circuit and package configuration are shown in Figure 19-22.

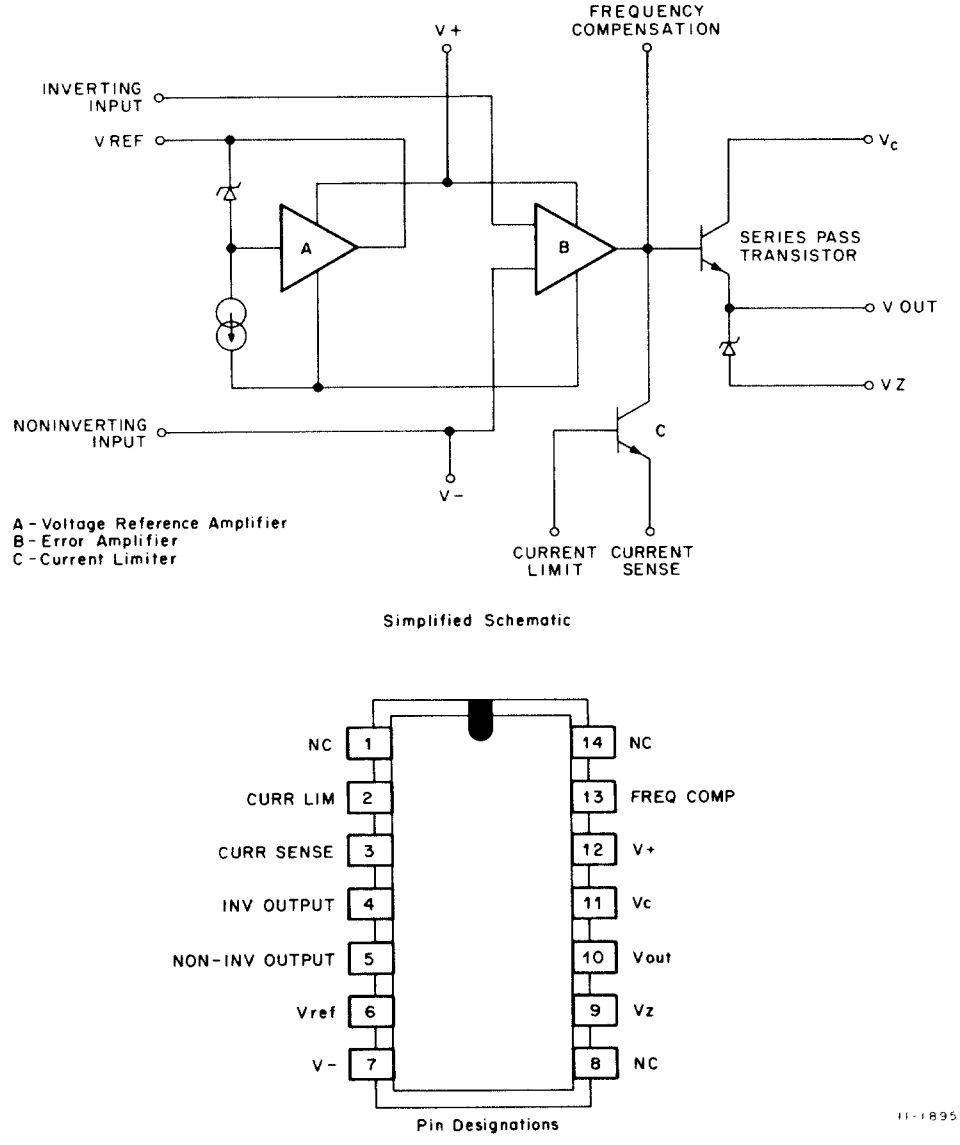


Figure 19-22 Voltage Regulator (E1) Equivalent Circuit and Package Configuration

The +5 V output passes through transistor Q2 to the output filter (C8, C9, and L1) and to the load. Q2 is called the pass transistor and is mounted on the heat sink. Transistor Q2 is operated in the switched mode; therefore, it is either on or off. It is controlled by drivers Q5, Q4, and Q3 that are controlled by voltage regulator E1. A simplified +5 V regulator circuit and associated waveforms are shown in Figure 19-23 to illustrate the operation of a switching regulator.

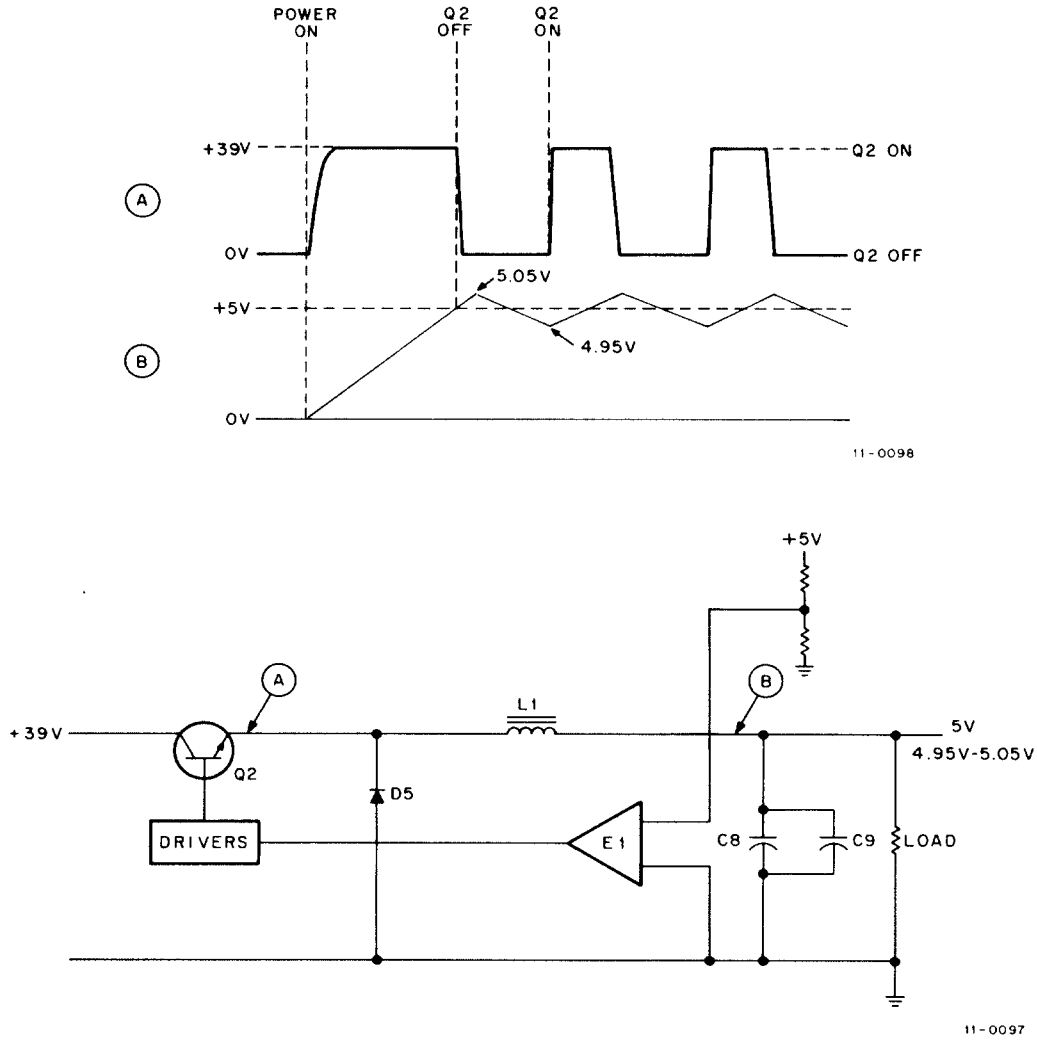


Figure 19-23 Simplified 5 V Switching Regulator Schematic and Waveforms

When power is applied, the drivers turn on Q2 and the output voltage starts to rise toward +39 V. Because of inductor L1 in the circuit, the voltage rise is relatively slow. When the output voltage reaches 5.05 V, E1 signals the drivers to cut off Q2. As the field associated with L1 starts to collapse, L1 current flows through the load to ground and returns to the other side of L1 through commutating diode D5, which is forward biased by the L1 back emf. The output voltage decays, and when it reaches 4.95 V, E1 signals the drivers to turn on Q2 and current is supplied through L1 to C8 and C9 and the load. The output voltage rises and when it reaches 5.05 V, E1 again signals the

drivers to cut off Q2. The circuit oscillates in this manner and generates a 39 V p-p rectangular pulse train across diode D5. The regulator circuit acts like a power Schmitt trigger and is either on or off depending on whether the output voltage is too low or too high. The filtered output across C8 and C9 is thus +5 V with about a 100 mV p-p 10 kHz nominal sawtooth of superimposed ripple. The output filter is an averaging device so the rectangular pulse train appears as an average voltage (+5 V nominal) at the output terminal.

If the load increases, the output voltage decays faster and Q2 turns on sooner so that the waveform frequency (duty cycle) increases. Conversely, if the load decreases, the waveform frequency (duty cycle) decreases.

The driving chain for Q2 consists of first stage driver Q3, predriver Q4, and off driver Q5, which is controlled by E1. Off driver Q5 diverts current from the base of Q4 and thus controls it. Q5, R2, and Zener diode D2 are used to generate +15 V for the operation of E1 from the +39 V raw input.

19.4.5.4 Overcurrent Protection Circuit – The regulator is protected from damage by high current due to a fault (short circuit) in the load. The current is limited to about 30 A by the overcurrent protection circuit that consists of Q1, R3 through R6, R25, R27, Q7, and C4.

The current drawn by the load through pass transistor Q2 is sensed by monitoring the voltage drop across 0.02 Ω resistor R4 that is in series with the +39 V raw voltage. If the current exceeds 30 A, the drop across R4 increases and forward biases Q1 and it turns on. Capacitor C4 charges and overcomes the bias on Q7 which turns it on. This action turns on E1 which, in turn, cuts off pass transistor Q2. The forward bias on Q1 is reduced and it turns off. Capacitor C4 discharges and holds E1 off for a period of time during which the current drops nearly to zero. When C4 discharges, E1 turns on to re-establish the output voltage. If the fault still exists, the overcurrent circuit turns off Q2 again. As long as the fault exists, the regulator oscillates in this mode and limits output current to approximately 30 A.

19.4.5.5 Overvoltage Crowbar Circuit – The +5 V is used to power digital logic devices that must be protected against voltage in excess of 7.0 V. This protection is provided by the overvoltage crowbar circuit that consists of silicon controlled rectifier D7, Zener diode D3, diode D8, Q6, R22, R23, and C7.

During normal operation, the trigger input to SCR D7 is at ground potential because the voltage across Zener diode is less than the 5.1 V required to cause it to conduct. If a malfunction occurs that increases the output voltage above 6.0 V, Zener D3 turns on which forward biases Q6. When Q6 conducts, resistor R23 in the SCR gate circuit draws current and turns on D7. The +5 V output is short circuited to ground. Capacitor C7 bypasses R23 to ground so that line transients of short duration that might cause D3 and D4 to conduct do not fire the crowbar.

19.5 POWER SUPPLY MAINTENANCE

19.5.1 Introduction

Power supply maintenance information includes the following items:

a. Checking and adjusting voltages
b. Removing power supply
c. Troubleshooting procedures

19.5.2 Checking and Adjusting Voltages

The power supply has four adjustable output voltages. Three voltages [+5 V (1), +15 V, and -15 V] are associated with the 5409728 DC Regulator and one [+5 V (2)] is associated with the H744 +5 V Regulator.

The computer must be extended more than half way out of the cabinet to provide access to all four adjustments. The three dc regulator adjustments are located in a vertical line midway on the right side of the computer; from top to bottom they are +15 V, +5 V and -15 V. The H744 Regulator adjustment is located on the bottom of the computer approximately 15 in. from the front and 1-1/2 in. from the right side. In each case, access is provided through holes in the computer mounting box and power supply chassis (Figure 19-24).

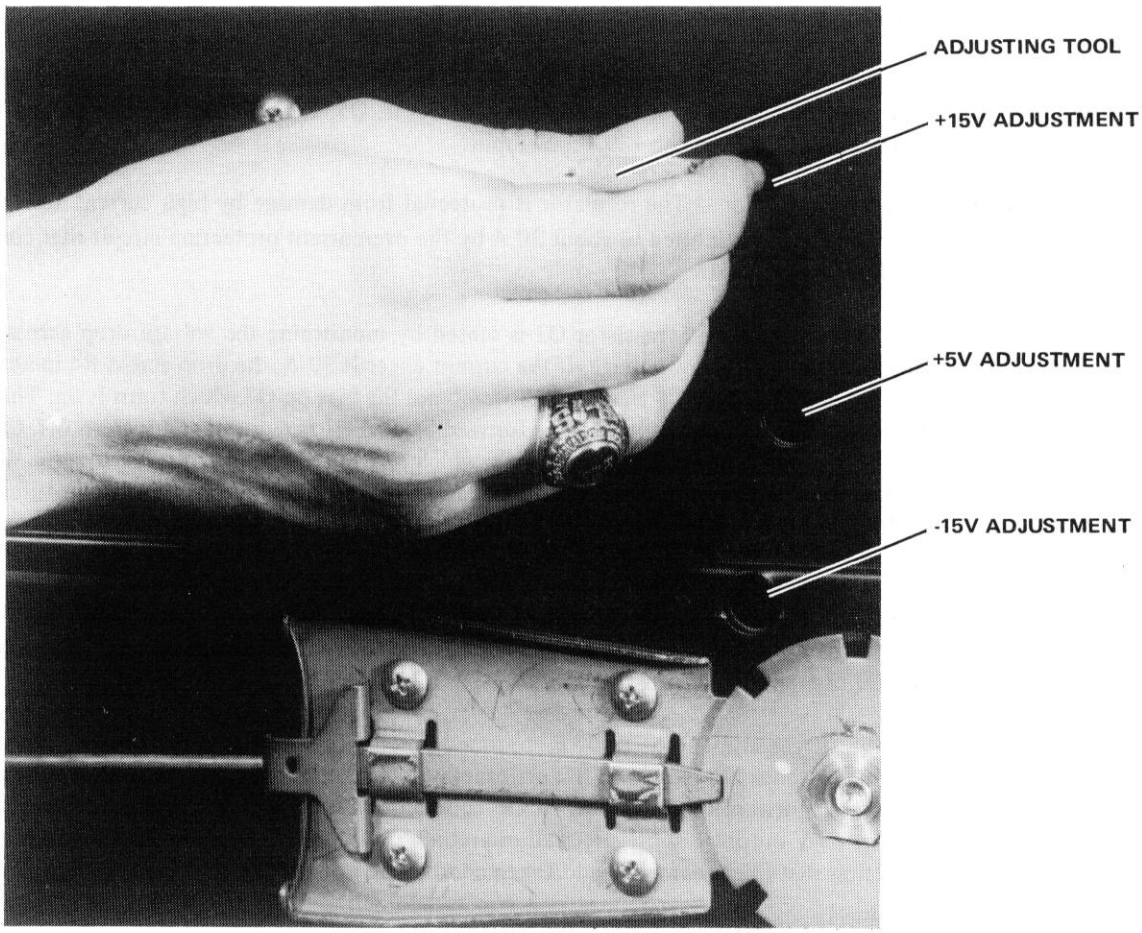


Figure 19-24 Power Supply Adjustments

All adjustments are controlled by potentiometers with slotted-head shafts that are conveniently rotated using a small blade type screw-driver. Clockwise rotation increases the voltage in each case. The output voltages should be checked and adjusted as close to nominal as possible. The nominal values and allowable tolerances are shown below.

5409728 Regulator Output Voltages

Nominal Value and Tolerance	Equivalent Range
5.0 V ± 5%	4.75 V to 5.25 V
15.0 V ± 5%	14.25 V to 15.75 V
-15.0 V ± 5%	-14.25 V to -15.75 V

H744 Regulator Output Voltage

Nominal Value and Tolerance	Equivalent Range
5.0 V ± 5%	4.75 V to 5.25 V

When adjusting the voltages, use a digital voltmeter and measure the output under load at the connectors (Faston tabs) on the pin side of the computer backplanes. These connectors are reached conveniently by extending the computer from the cabinet, locking it in the 90° front up position and removing the bottom cover.

Observe the following cautions when adjusting the output voltages.

1. Do not adjust the voltages beyond the 105% rating to avoid activating the overvoltage protection (crowbar) circuit. In the case of the H744 Regulator, the +5 V output is drastically reduced when the crowbar fires but the fuse does not blow. In the case of the 5409728 Regulator, fuse F1 (15 A) blows if the +5 V output is adjusted too high; and fuse F2 (10 A) blows if the -15 V output is adjusted too high. These crowbar circuits are designed to blow the fuses when activated. The +15 V output has no overvoltage protection circuit but it uses fuse F1 for protection in case of a malfunction in the +15 V supply.

2. The two +5 V outputs, +5 V(1) from the 5409728 Regulator and +5 V(2) from the H744 Regulator, must not be shorted together. Output +5 V(1) is available on power distribution board connectors J1 and J2; and output +5 V(2) is available on connectors J3, J4, and J5 of this board.

19.5.3 Power Supply Removal

The following procedure must be used to prevent damage to the power supply during removal from the mounting box:

1. Turn off power.

2. Remove the two screws that hold the line set to the rear of the mounting box, withdraw the line set slowly, and disconnect line set connector J5 from power supply harness connector H1-P1 (Figure 19-25).

3. Remove the six screws on the right side of the mounting box that hold the power supply chassis to the mounting box (Figure 19-26). Disconnect the console cable connector from the Berg connector on the M7260 module and move the cable away from the power supply cover. Remove the four screws that secure the cover and remove it from the power supply.

4. Disconnect the following connectors that are accessible at the rear of the power supply (Figure 19-27).

   a. Power Supply harness connector H1-J2 from power distribution harness connector H2-P3.

   b. Power distribution harness connector H2-P2 from transformer connector T2-J1 (2 red and 2 black wires).

CAUTION

The dc regulator output connector PS1-J2 is still connected but it is not accessible.

5. Lift the power supply chassis slowly upward until it is free of the compartment in the mounting box (Figure 19-28). Rest the bottom of the power supply chassis on the top of the mounting box and remove power distribution harness connector H2-P1 from dc regulator output connector PS1-J2 (Figure 19-29).

6. Place the power supply on a bench. Be careful when lifting and carrying the power supply because its center of gravity is near the front end.

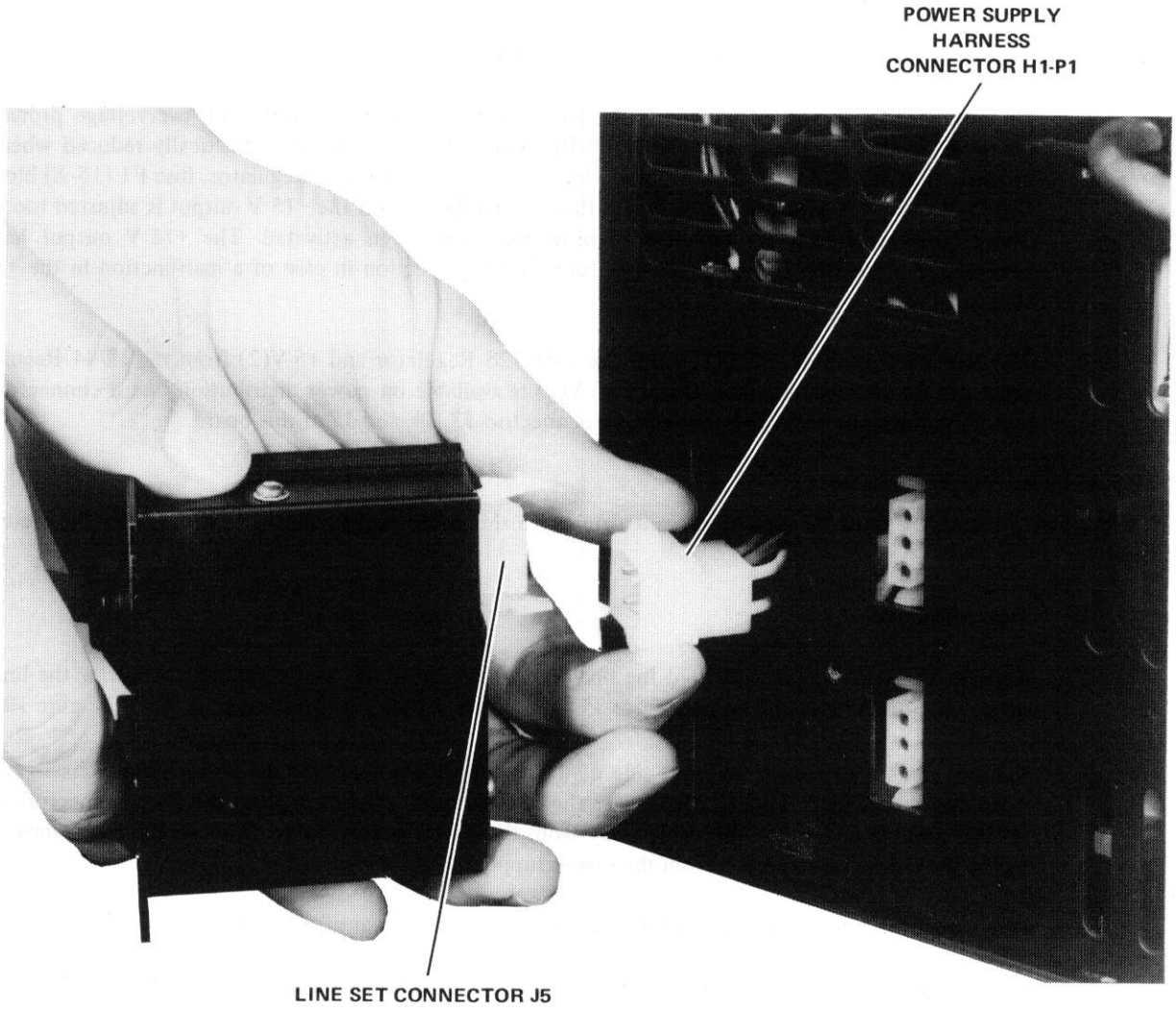


Figure 19-25 Disconnecting Line Set From Power Supply

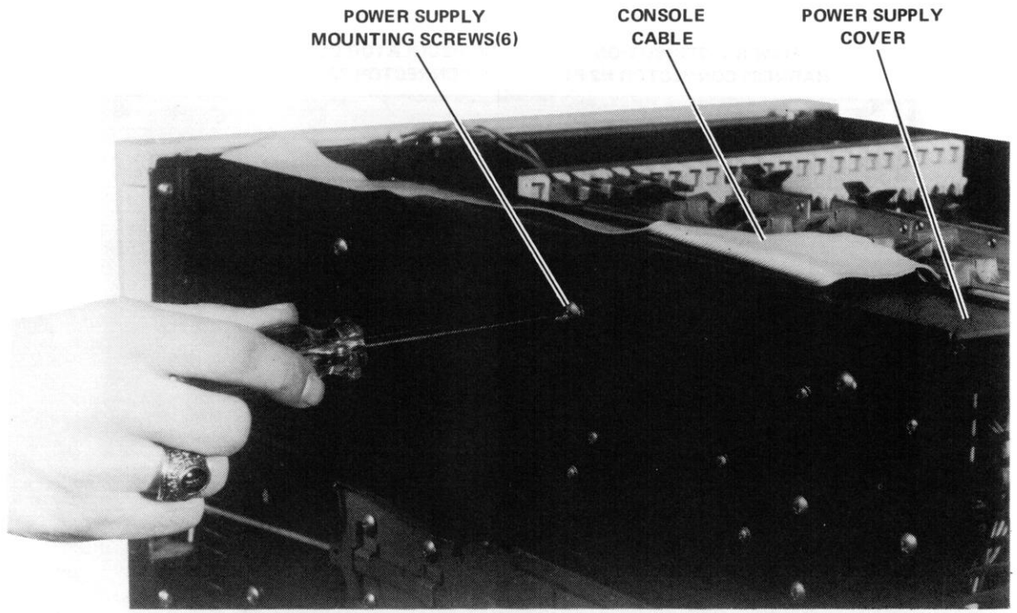


Figure 19-26 Removing Power Supply Mounting Screws

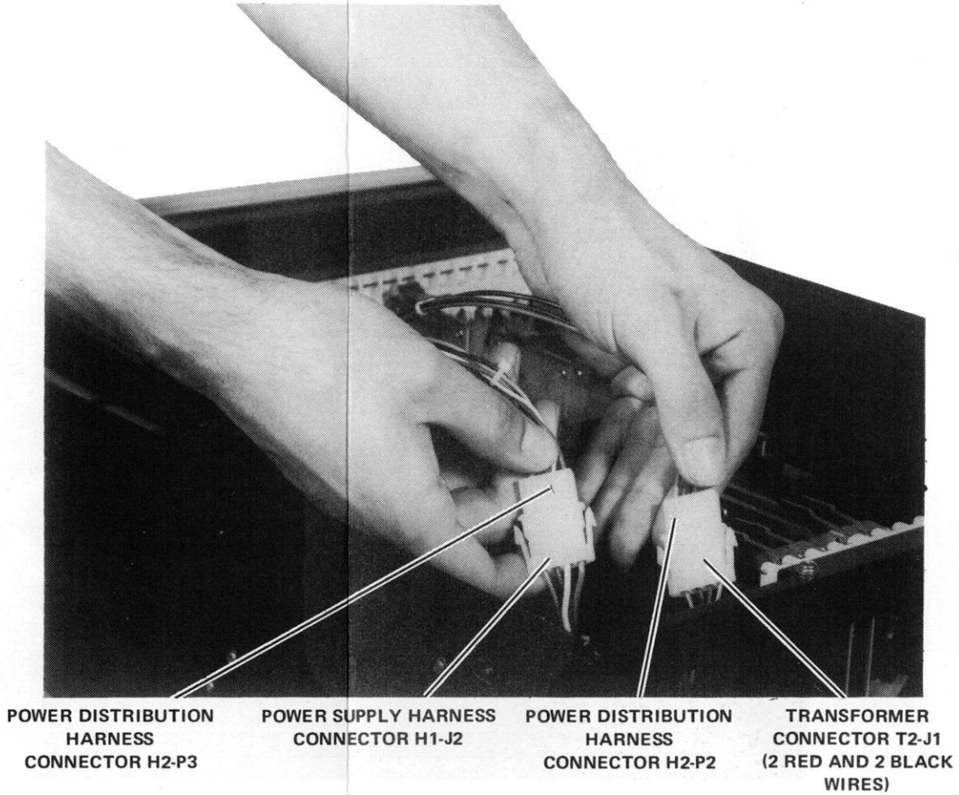


Figure 19-27 Removing Power Distribution Harness Connectors H2–P2 and H2–P3

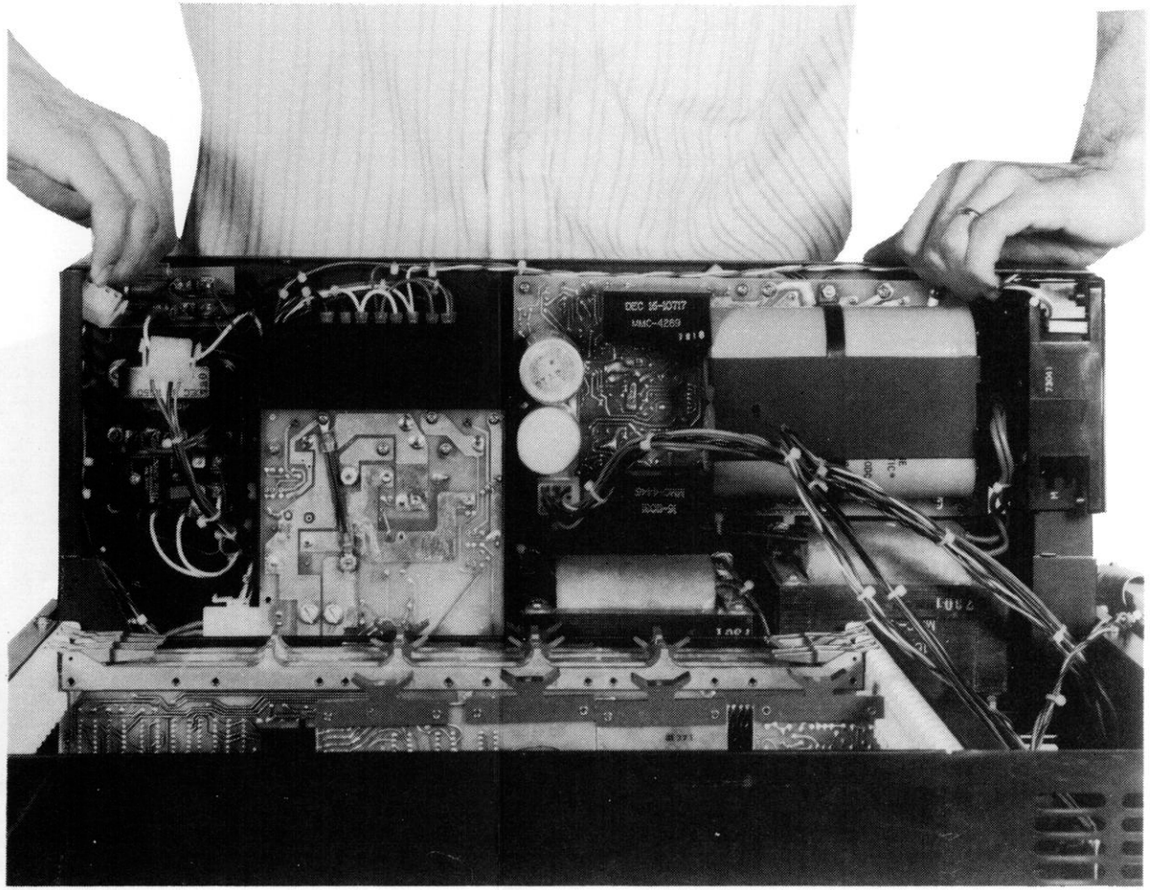


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Figure 19-28 Lifting Power Supply
From Mounting Box

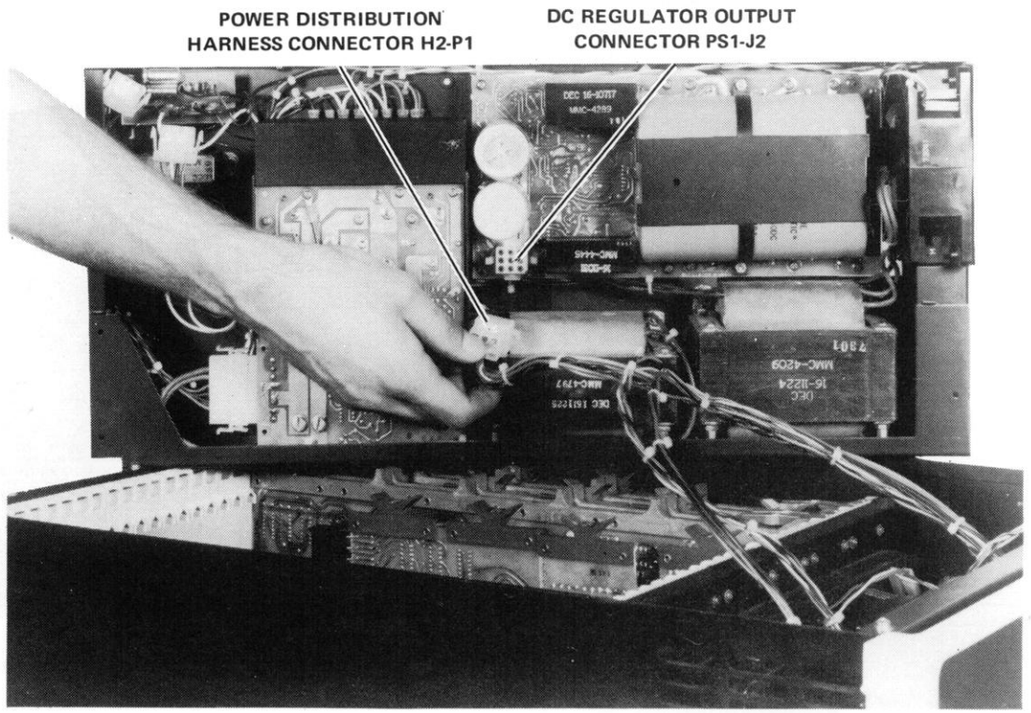

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Figure 19-29 Disconnecting DC
Regulator Output Connector

19.5.4 Troubleshooting Procedures

19.5.4.1 Introduction – Most of the troubleshooting information presented relates to the components 5409728 Regulator and H744 Regulator.

Troubleshooting the other power system components such as the line set, relay, transformers, connectors, etc., can be accomplished by performing an electrical continuity check using the power system interconnection diagram (Figure 19-10).

19.5.4.2 Troubleshooting Hints

WARNING

Dangerous voltages (115 or 230 Vac) are present in the power system. Be careful when servicing these circuits.

Because of the physical configuration of the power supply, very little troubleshooting can be performed with the power supply installed. Voltages can be checked under load on the pin side of the computer backplane. For some malfunctions, the problem can be isolated to the load or power supply by disconnecting the backplane cable and checking the power supply outputs at the power distribution board connectors. Refer to the power distribution board circuit schematic (Figure 19-13) and list of signals (Table 19-2).

The most likely source of a power supply malfunction is the 5409728 Regulator or the H744 Regulator. A quick remedy for a malfunction in either of these regulators is to replace the complete unit. The replacement regulator may need adjustment to compensate for the load. If the new regulator is initially adjusted too high, it may activate the crowbar circuit. In the case of the H744 Regulator, no output is generated. In the case of the 5409728 Regulator, no output is generated and the +5 V fuse or −15 V fuse blows. If this should happen, remove power and rotate the appropriate voltage adjustment fully counterclockwise. Replace the fuse, if required, and apply power. Adjust the output to the recommended value per Paragraph 3.5.2.

NOTE

When replacing or swapping the 5409728 DC Regulator (PS1), etch revision D or later must be used. Earlier etch revisions, such as revision C which is used in the 5-1/4 in. PDP-11/05, 11/10 Computer, must not be installed because of insufficient current capacity.

19.5.4.3 Troubleshooting the 5409728 Regulator – Table 19-4 is a troubleshooting chart for the 5409728 Regulator. It should be used with Figures 19-15 through 19-19 or regulator schematic drawing D-CS-5409728-0-1 in the print set.

A visual check is a valuable aid in locating the cause of a malfunction. Check for loose connections, burned resistors, burned printed circuit board etch, cracked transistors or leaky capacitors.

As an additional aid to troubleshooting the 5409728 Regulator, waveform photos are provided for the +5 V and −15 V outputs. These waveforms were taken on a Tektronix Model 453 Oscilloscope. All waveforms are with respect to power common (J2 pin 2).

Table 19-4
5409728 Regulator Troubleshooting Chart

Problem	Cause
No +5 V and +15 V output	F1 open D14 or transformer T1 open +5 V adjusted too high*
+5 V Output Too Low	Q5, D9, Q10, Q9, Q11, D12, or D10 shorted C5 or C7 shorted R49, R50, R46, or R44 open Q6, Q7, Q8, or D11 shorted Q9, Q10, or D9 open* R51 or R50 open
+15 V Output Too High	Q1 shorted D8 open R35 or R36 open
No -15 V Output	F2 open D14 or transformer T1 open
-15 V Output Too Low	-15 V adjusted too high* Q25, D4, Q26, Q21, Q27, D7, or D5 shorted C14 or C12 shorted R22, R26, R25, or R29 open Q22, Q23, Q24, or D6 shorted Q25, Q26, or D4 open
BUS AC LO L Will Not Go High	Q13, Q14, or Q15 shorted Q16 or D3 open R7, R3, R6, or R8 open C9 shorted
BUS AC LO L Will Not Go Low and/or acts erratically on poweron/poweroff	Q13, Q14, or Q16 open Q15 or D3 shorted R12, R13, R7, or R10 open
BUS DC LO L Will Not Go High	Q19, Q20, or Q18 shorted Q17 or D3 open R7, R2, or R6 open C9 shorted
BUS DC LO L Will Not Go Low	Q19, Q20, or Q17 open Q18 or D3 open R7, R3, or R6 open C9 shorted

Table 19-4 (Cont)
5409728 Regulator Troubleshooting Chart

Problem	Cause
BUS DC LO L Will Not Go Low and/or acts erratically on poweron/poweroff	Q19, Q20, or Q17 open Q18 or D3 shorted R9, R10, R11, or R8 open
No LTC L Signal	R55 open D13 shorted
LTC L Going Too High	D13 open

*These causes make the crowbar fire, which, in turn, blows the appropriate fuse.

Figure 19-30 shows six waveforms for the +5 V output taken at points A and B in the circuit (Figure 19-18). Point A is the output of pass transistor Q6 and point B is the +5 V output (J2 pin 3). Waveforms a, b, and c are taken at point A and waveforms d, e, and f are taken at point B. Figure 19-31 shows six waveforms for the -15 V output taken at points C and D in the circuit (Figure 19-19). Point C is the output of pass transistor Q22 and point D is the -15 V output (J2 pin 9). Waveforms a, b, and c are taken at point C and waveforms d, e and f are taken at point D.

19.5.4.4 Troubleshooting the H744 Regulator – The design of the +5 V H744 Regulator is similar to the +5 V portion of the 5409728 Regulator. In general, the same troubleshooting procedures and fault isolation techniques apply to both regulators.

Some specific troubleshooting procedures are listed for the H744. Refer to Figure 19-21 which is the H744 circuit schematic.

a. A regulator that provides no output, or low output, without causing fuse F1 to blow is probably working into a short-circuited output. Check for a short circuit in the load or a component failure in the crowbar circuit.

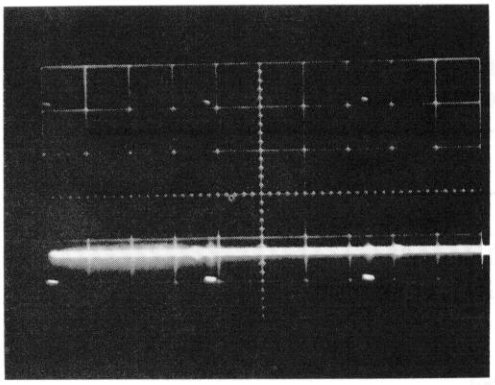
b. A regulator that provides no output and has fuse F1 blown usually indicates a fault in the pass transistor or its driver network. Proceed as follows:

   1. Check for scorching of the etched board in the area of Q3 and Q4. Check the associated base-emitter bleeder resistors for damage.

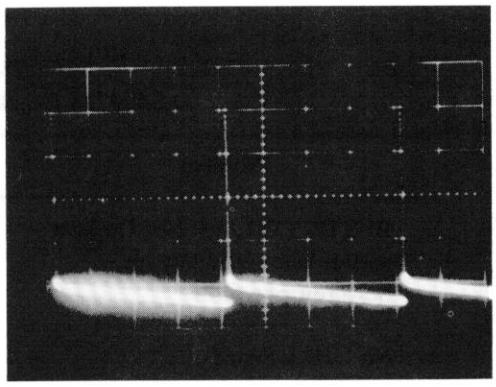
   2. Check pass transistor Q2, drive transistors Q3 and Q4, and level shifter Q5 with an ohmmeter. The fault could be caused by continuous base drive to Q4.

   3. The fault could be caused by an external short-circuit that holds precision voltage regulator E1 in conduction. E1 pin 4 to ground should measure approximately 20K Ω. E1 pin 5 to ground should measure approximately 1.5K Ω.

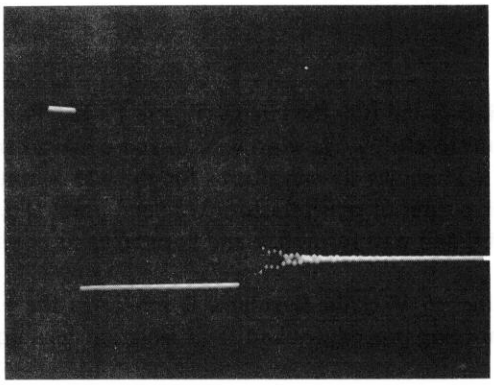
   4. Check for shorts to ground at the fuse terminals and components mounted on the heat sink.



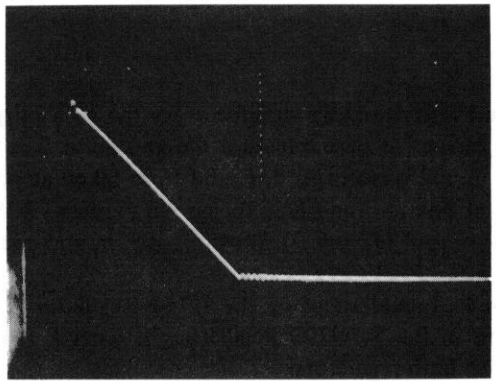
a) Point A, No load,
2 ms /div, and
10V/div.



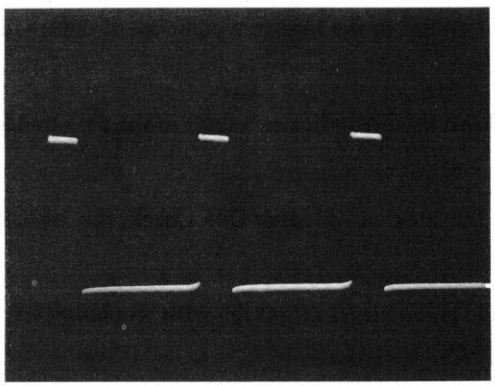
d) Point B, No load,
2 ms/div, and
50 mV/div.



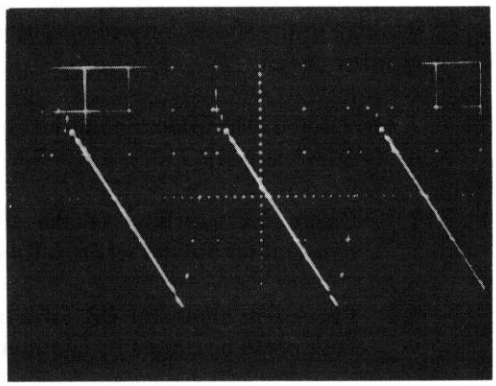
b) Point A, No load,
20 μs/div, and
10V/div.



e) Point B, No load,
20 μs/div, and
50 mV/div.

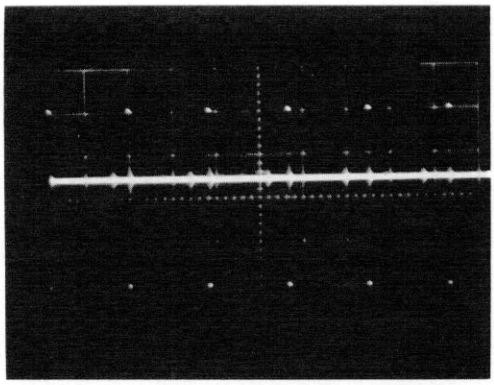


c) Point A, 20A load,
20 μs/div, and
10V/div.

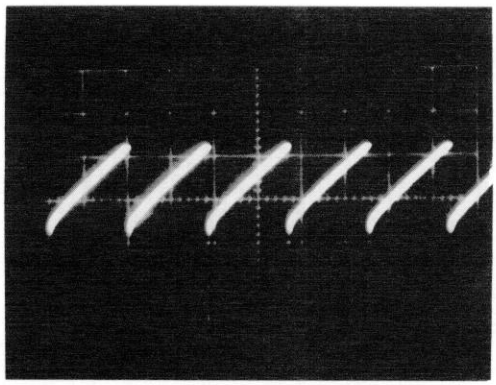


f) Point B, 20A load,
μs/div, and
50 mV/div.

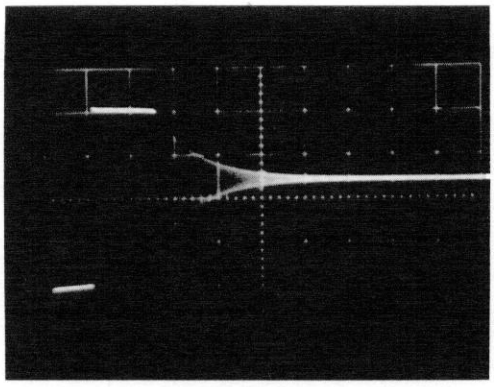
Figure 19-30 +5 V Regulator Circuit Waveforms



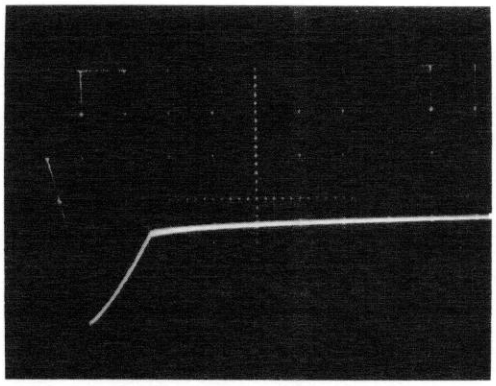
a) Point C, No load,
5 ms/div, and
10V/div.



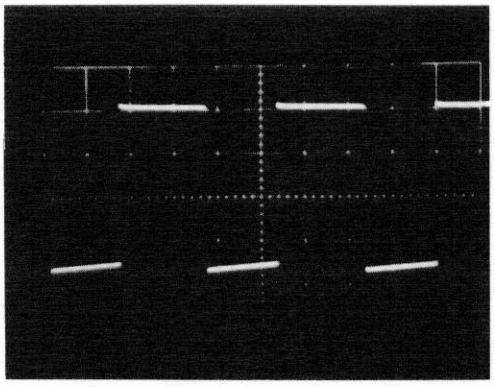
d) Point D, No load,
5 ms/div, and
50 mV/div.



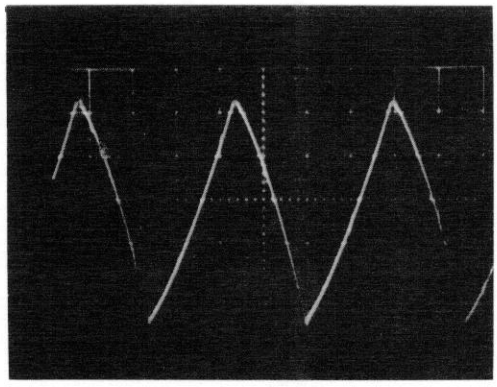
b) Point C, No load,
50 μs/div, and
10V/div.



e) Point D, No load,
50 μs/div, and
50 mV/div.



c) Point C, 5A load,
50 μs/div, and
10V/div.



f) Point D, 5A load,
50 μs/div, and
50 mV/div.

Figure 19-31 −15 V Regulator Circuit Waveforms

APPENDIX A
INTEGRATED CIRCUIT DESCRIPTIONS

A.1 INTRODUCTION

The MSI and LSI integrated circuits (ICs) which are shown in the engineering drawings are discussed in the following paragraphs. The descriptions include a pin location diagram, simplified logic diagram, and truth table. These descriptions are intended as maintenance aids for troubleshooting to the IC level. Table A-1 lists the ICs by part number, name, and respective paragraph number.

Table A-1
Integrated Circuits

Manufacturer Part Number	DEC Part Number	Name	Para.
8266	19-09934	2-Input, 4-Bit Digital Multiplexer	A.2
7413	19-09989	Dual NAND Schmitt Triggers	A.3
7473	19-05587	Dual J-K Master-Slave Flip-Flops	A.4
7474	19-05547	Dual D-Type, Edge-Triggered Flip-Flops	A.5
7475	19-09050	4-Bit Bistable Latch	A.6
7489	19-10396	64-Bit Read/Write Memory	A.7
74121	19-10230	Monostable Multivibrator	A.8
74150	19-10153	Data Selector Multiplexer	A.9
74153	19-09927	Dual 4-Line-to-1-Line Data Selectors/Multiplexers	A.10
74154	19-09701	4-Line-to-16-Line Decoders/ Demultiplexers	A.11

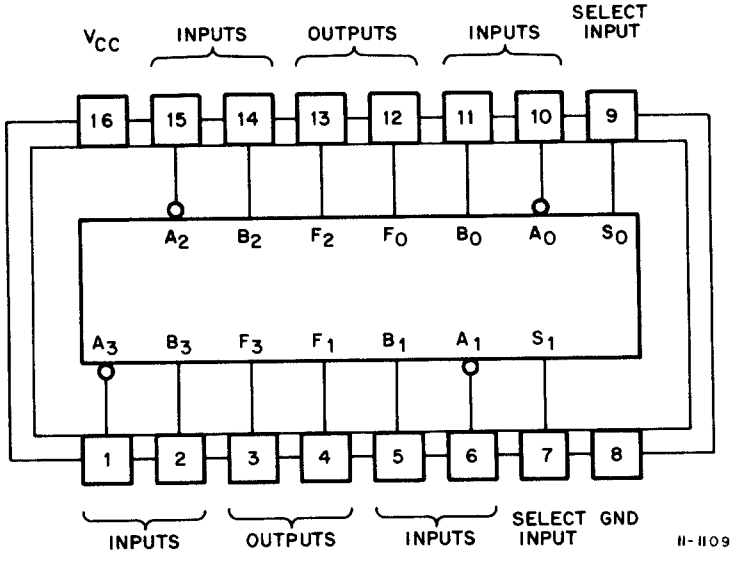
Table A-1 (Cont)
Integrated Circuits

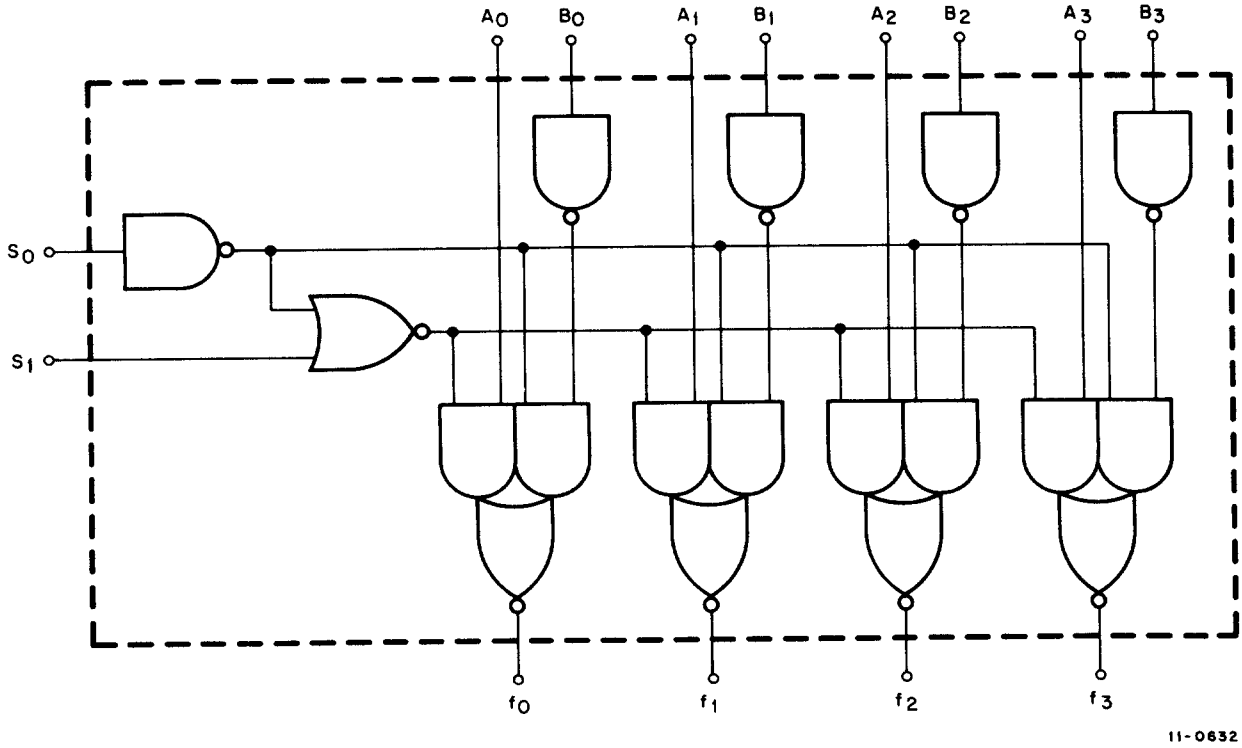
Manufacturer Part Number	DEC Part Number	Name	Para
74157/74S158	19-10655/ 19-10656	Quadruple 2-Line-to-1-Line Multiplexer	A.12
74174/74175	19-10652/ 19-10651	D-Type Flip-Flops, Hex/Quad with Clear	A.13
74181	19-09982	Arithmetic Logic Unit/Function Generator (ALU)	A.14
74182	19-10019	Look-Ahead Carry Generator	A.15
74193	19-10018	Synchronous 4-Bit Up/Down Counter (Dual Clock with Clear)	A.16
74194	19-10623	4-Bit Bidirectional Universal Shift Registers	A.17
7528	19-10687	Dual Sense Amplifiers with Preamplifier Test Points	A.18
9602	19-09374	Dual Retriggerable Monostable Multivibrator with Clear	A.19

A.2 8266 2-INPUT, 4-BIT DIGITAL MULTIPLEXER

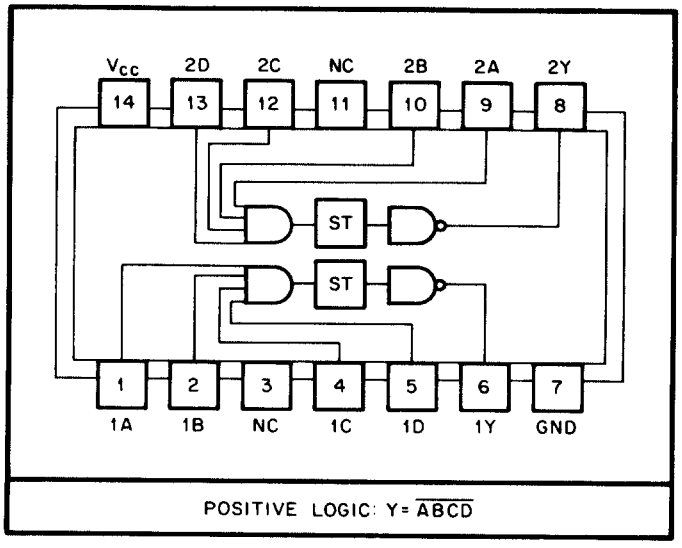
Truth Table

Select Lines		Output
S_0	S_1	t_n (0,1,2,3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1



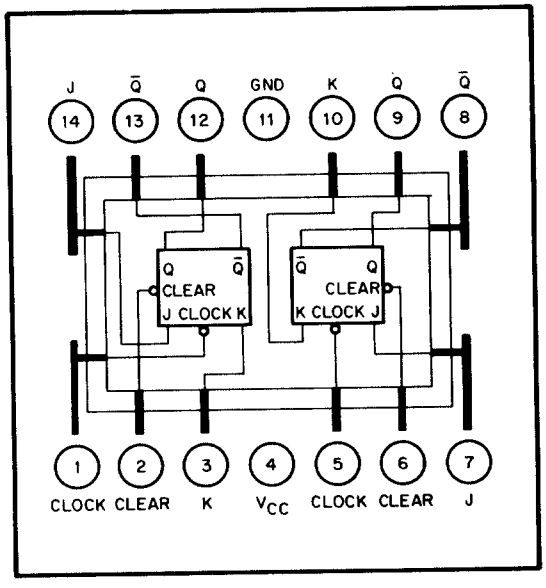


A.3 7413 DUAL NAND SCHMITT TRIGGERS



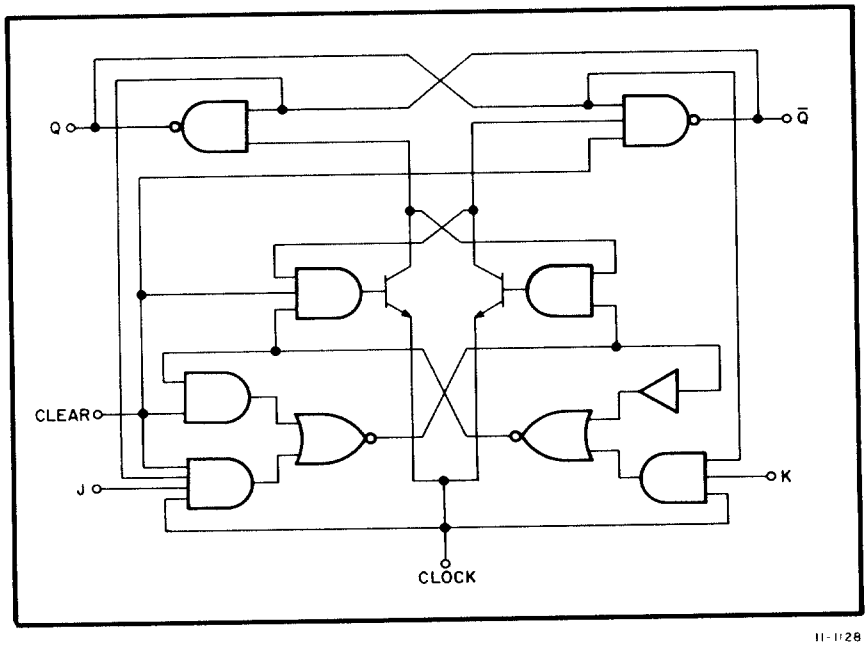
11-1114

A.4 7473 DUAL J-K MASTER-SLAVE FLIP-FLOPS



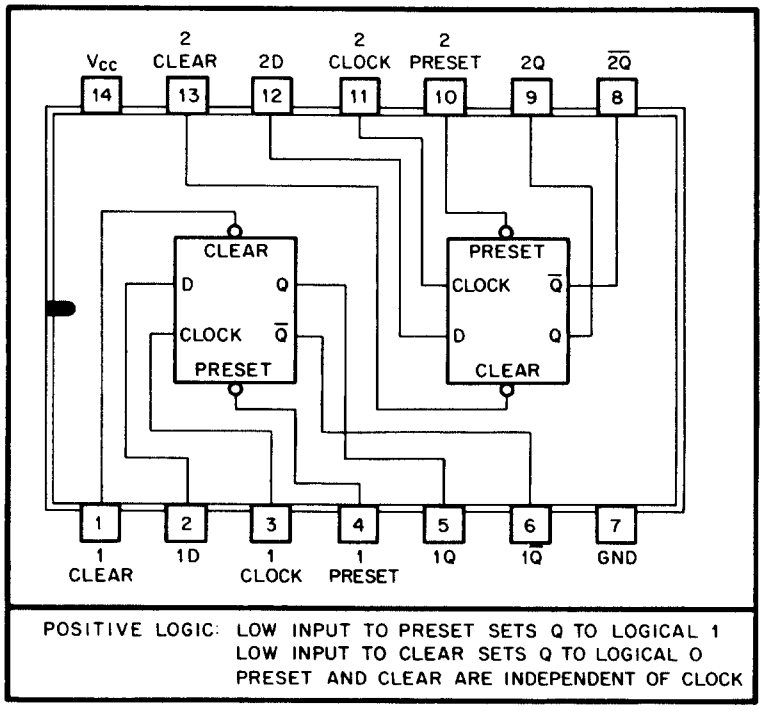
TRUTH TABLE (EACH FLIP-FLOP)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.



11-1128

A.5 7474 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS



11-0766

Truth Table (Each Flip-Flop)

t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
0	0	1
1	1	0

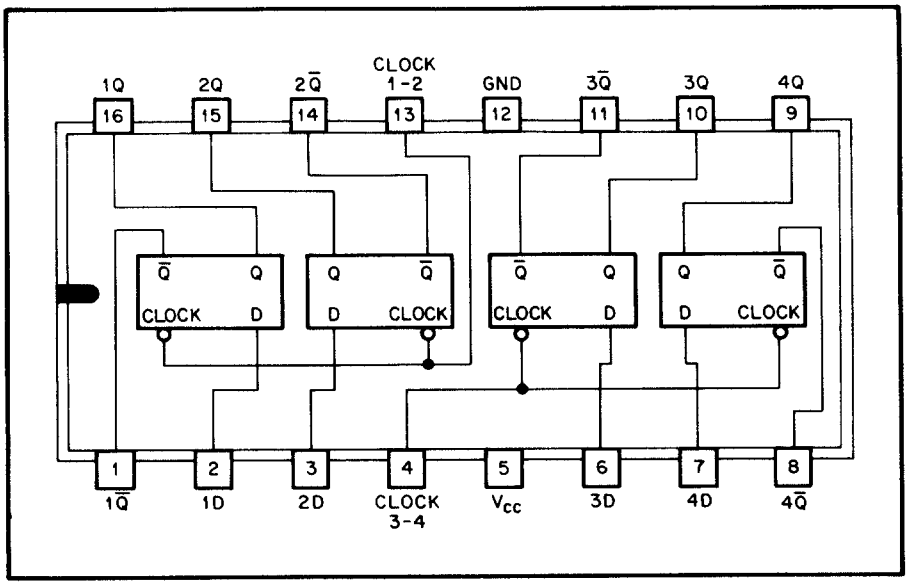
Notes: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

A.6 7475 4-BIT BISTABLE LATCH

Truth Table
(Each Latch)

t_n	t_{n+1}
D	Q
1	1
0	0

NOTES:
1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

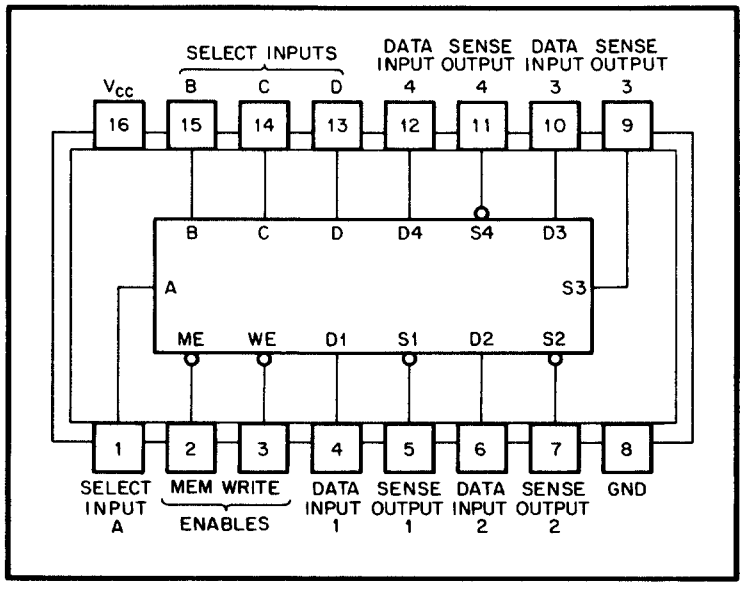


11-0894

A.7 7489 64-BIT READ/WRITE MEMORY

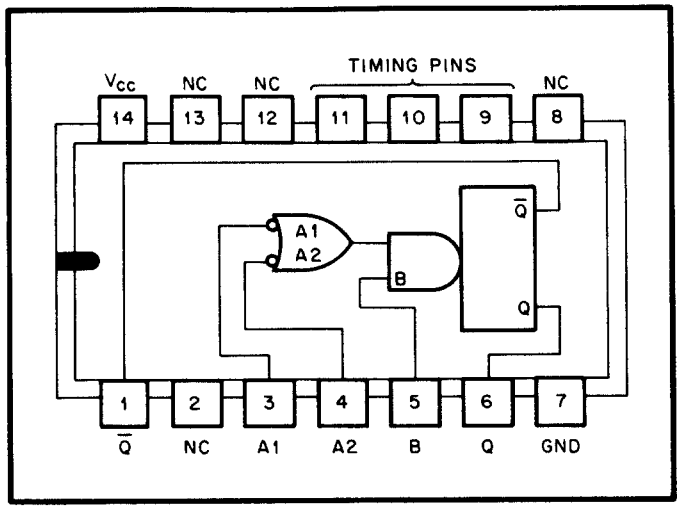
Function Table

ME	WE	Operation	Condition of Outputs
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High



11-1117

A.8 74121 MONOSTABLE MULTIVIBRATOR



11-1119

TRUTH TABLE

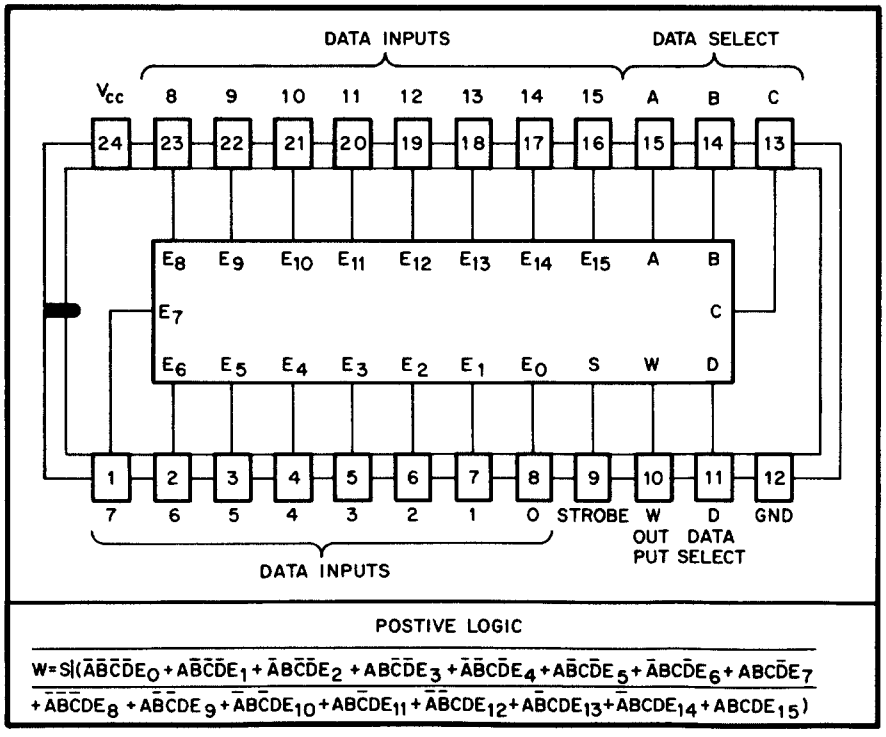
t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	1	0	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

1 = $V_{in(1)} \geq 2V$

0 = $V_{in(0)} \leq 0.8V$

A.9 74150 DATA SELECTOR MULTIPLEXER

DUAL-IN-LINE PACKAGE (TOP VIEW)



POSTIVE LOGIC

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7 + \bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

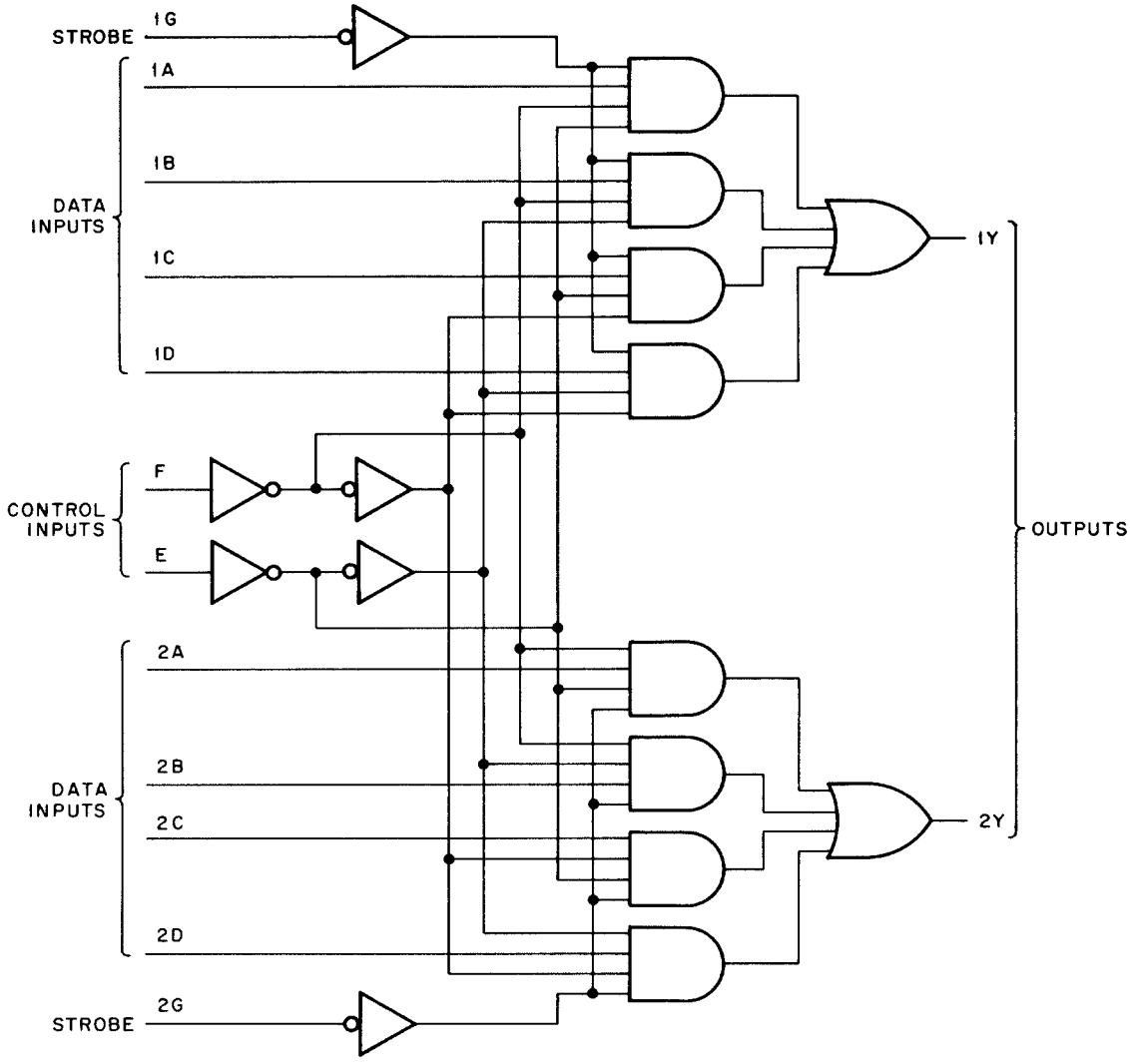
12-0324

TRUTH TABLE

Inputs																				Output
D	C	B	A	Strobe	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1
0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1
0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
0	0	0	1	0	x	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1
0	0	0	1	0	x	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
0	0	1	0	0	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x	x	1
0	0	1	0	0	x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	x	0
0	0	1	1	0	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x	1
0	0	1	1	0	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	0
0	1	0	0	0	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	1
0	1	0	0	0	x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	0
0	1	0	1	0	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x	1
0	1	0	1	0	x	x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	0
0	1	1	0	0	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x	1
0	1	1	0	0	x	x	x	x	x	x	1	x	x	x	x	x	x	x	x	x	0
0	1	1	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1
0	1	1	1	0	x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	x	0
1	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	1
1	0	0	0	0	x	x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	0
1	0	0	1	0	x	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	1
1	0	0	1	0	x	x	x	x	x	x	x	x	x	1	x	x	x	x	x	x	0
1	0	1	0	0	x	x	x	x	x	x	x	x	x	x	0	x	x	x	x	x	1
1	0	1	0	0	x	x	x	x	x	x	x	x	x	x	1	x	x	x	x	x	0
1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x	x	1
1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	1	x	x	x	x	0
1	1	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x	1
1	1	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	1	x	x	x	0
1	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	1
1	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	1	x	x	0
1	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	x	1
1	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	x	0
1	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	1
1	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	0

When used to indicate an input condition, x = logical 1 or logical 0.

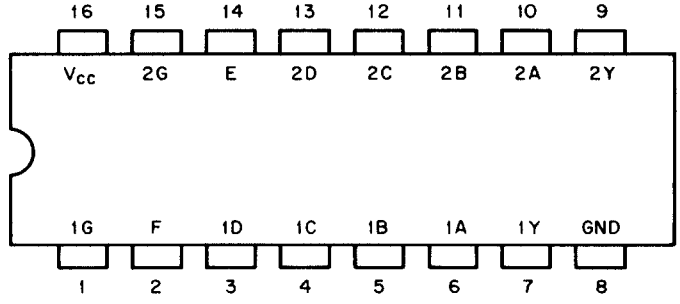
A.10 74153 DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS



LOGIC DIAGRAM

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)

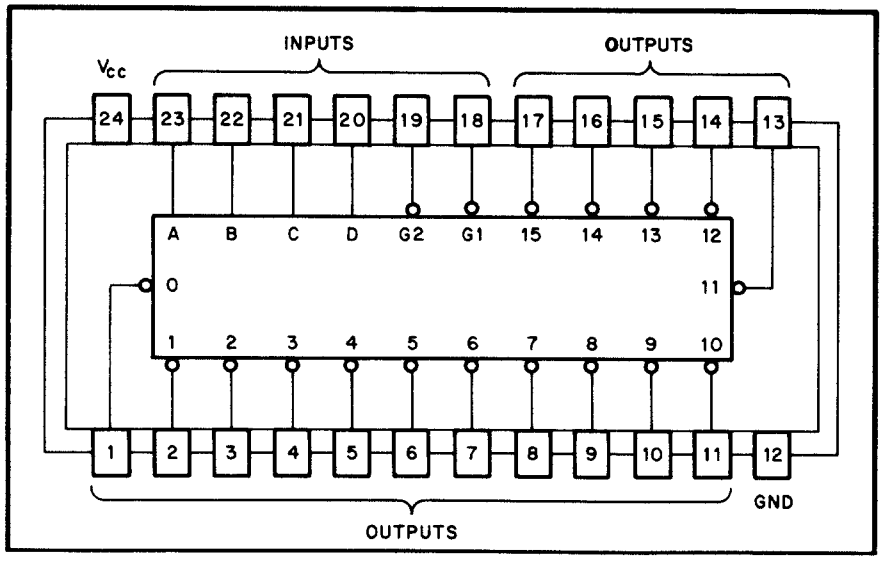


PIN LOCATOR
(TOP VIEW OF IC)

8E-0138

A.11 74154 4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

DUAL-IN-LINE PACKAGE (TOP VIEW)



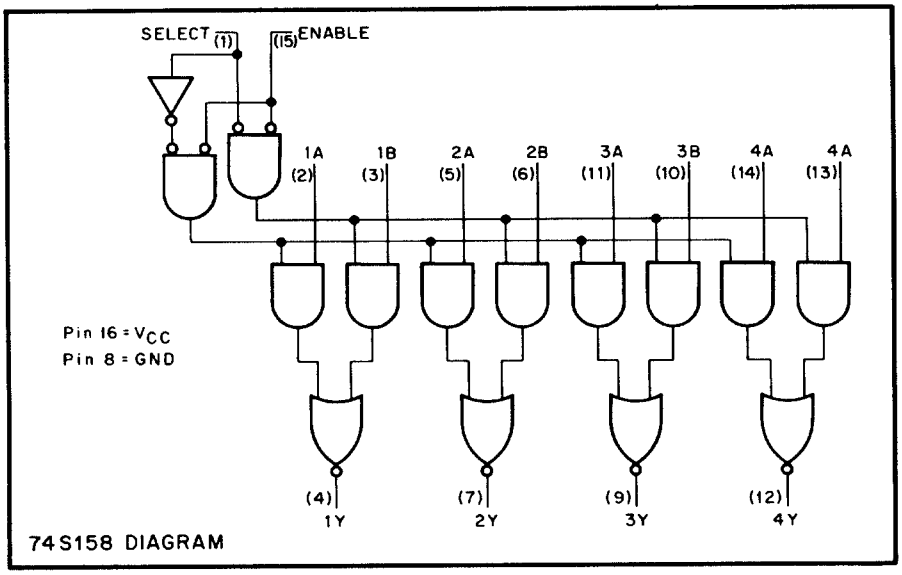
II-0636

TRUTH TABLE

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high, L = low, X = irrelevant

A.12 74157/74S158 QUADRUPLE 2-LINE-TO-1-LINE MULTIPLEXER

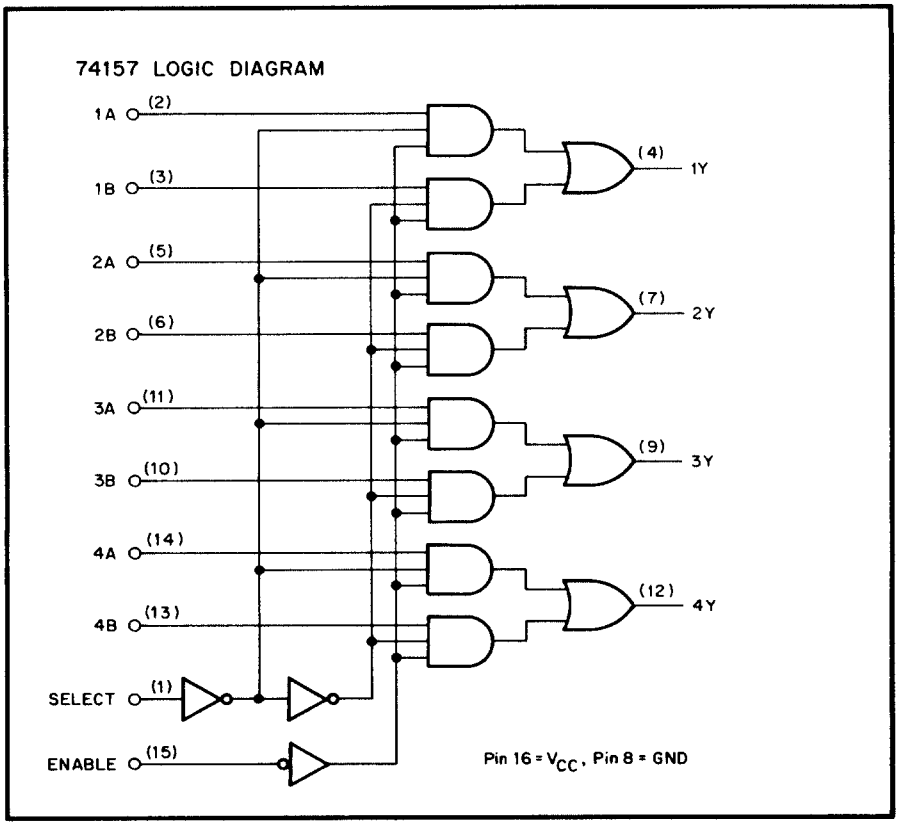


74S158 DIAGRAM

TRUTH TABLE

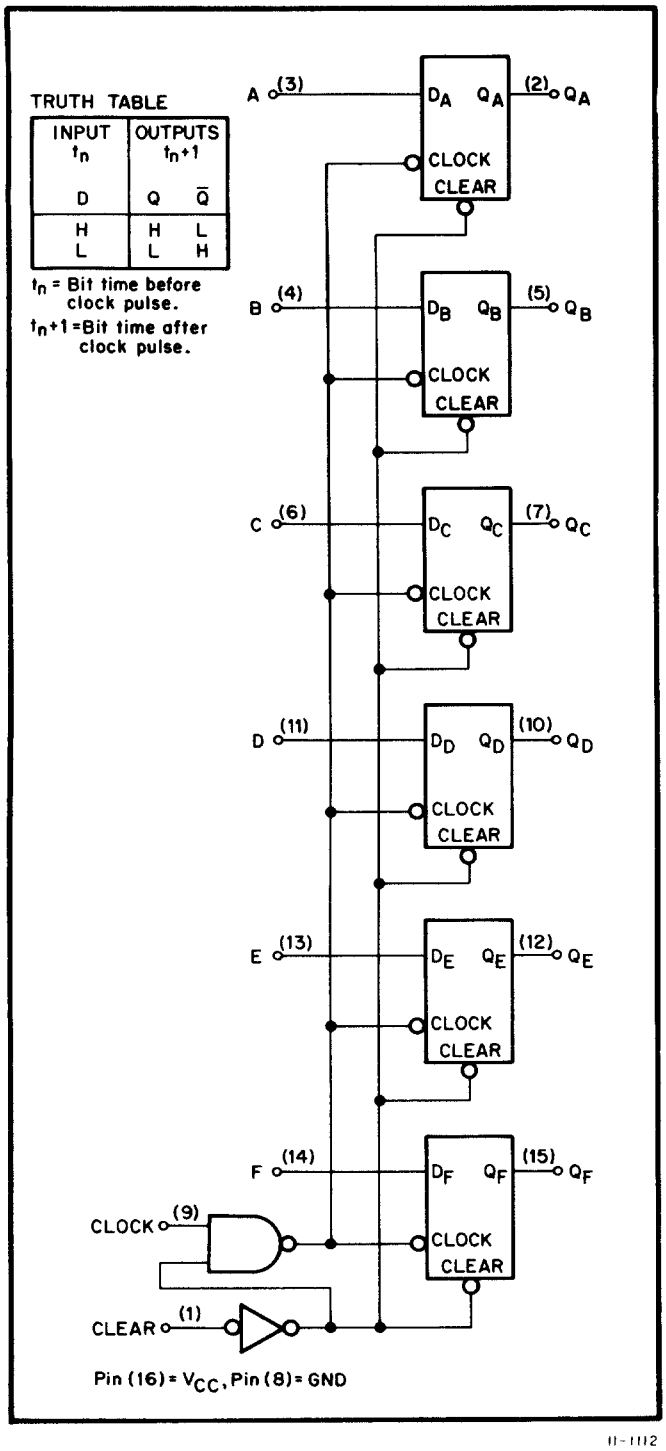
INPUTS			OUTPUT Y	OUTPUT W
ENABLE	SELECT	A B	74157	74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

H = High level, L = Low level, X = Irrelevant

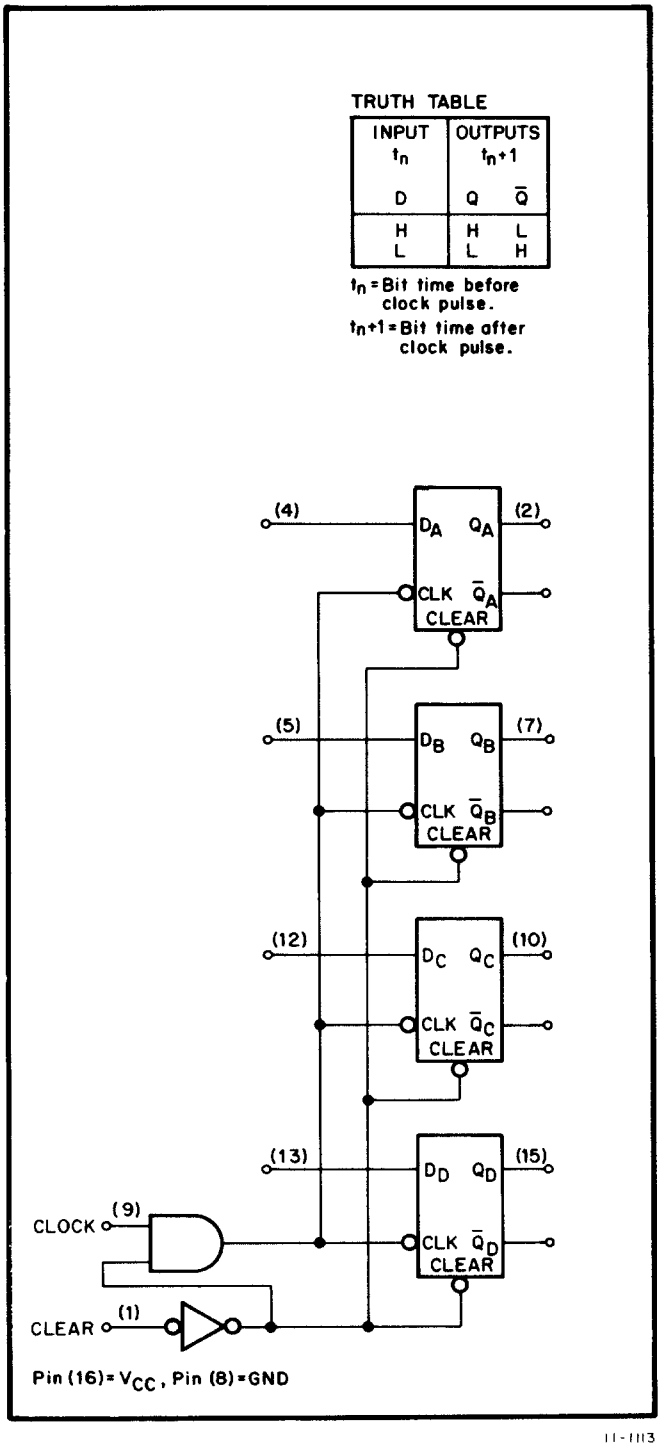


TL/F/11131

A.13 74174 HEX/74175 QUAD D-TYPE FLIP-FLOPS WITH CLEAR



74174 Diagram



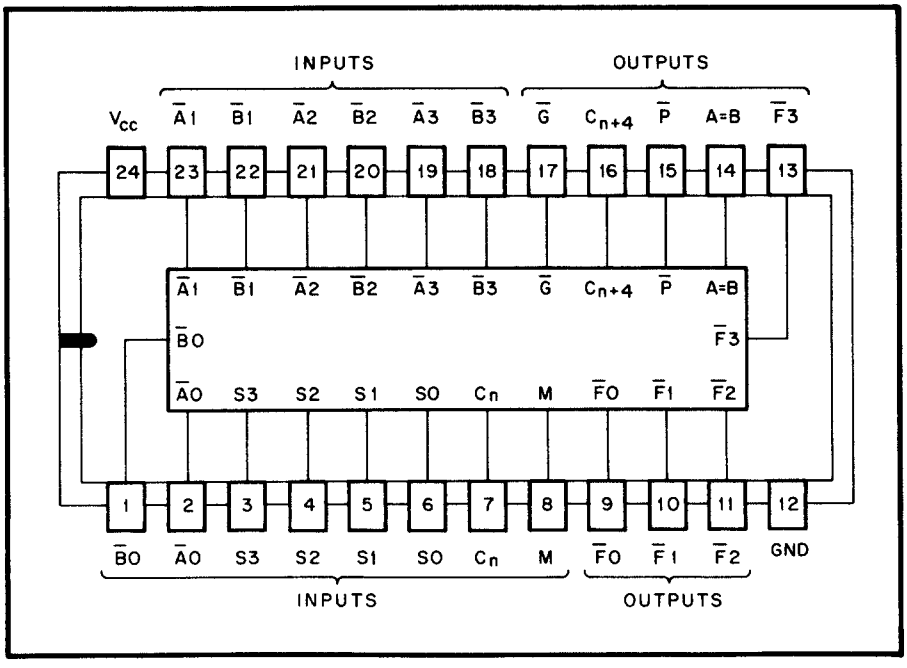
74175 Diagram

A.14 74181 ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR (ALU)

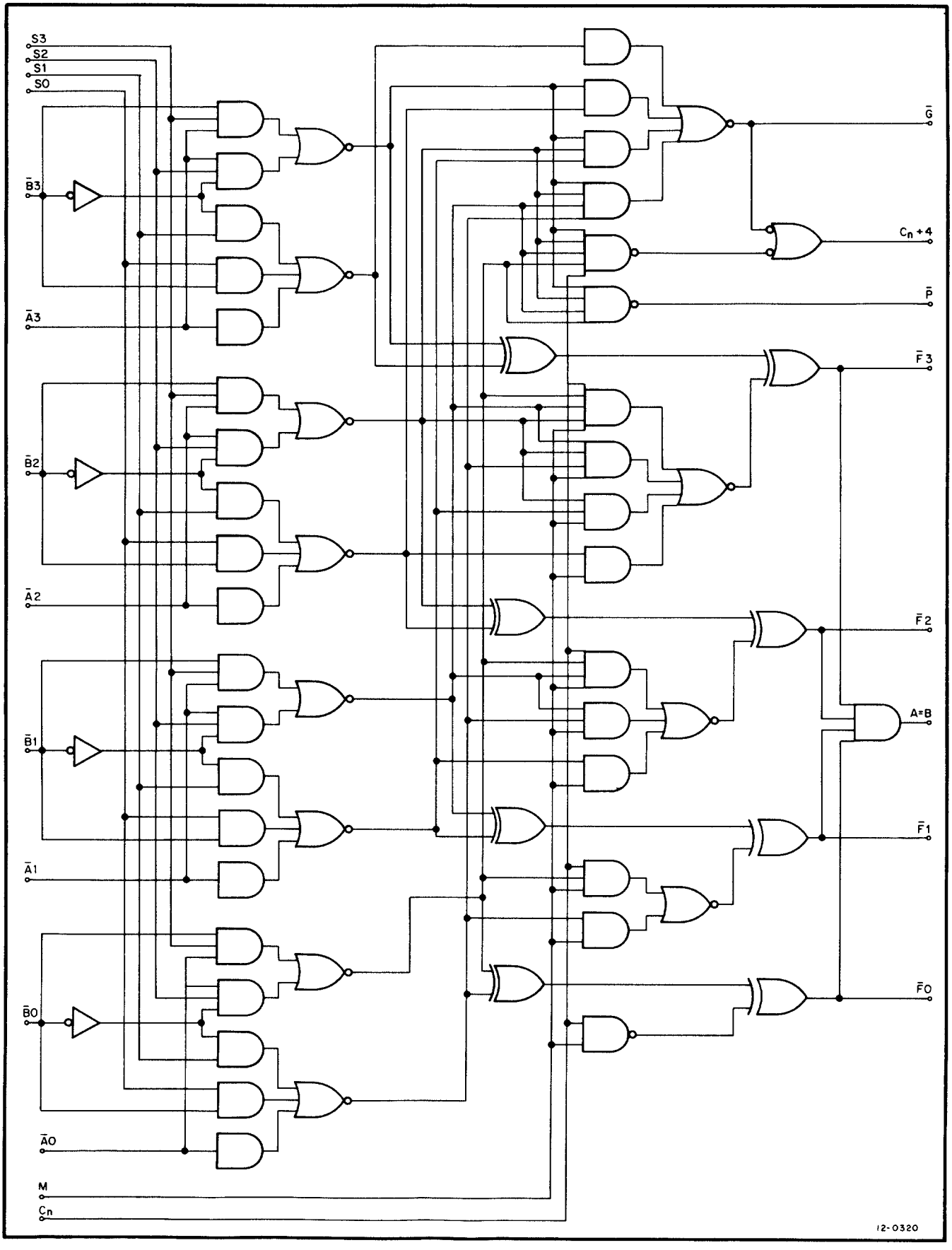
Selection				Active-Low Data		
				M = H	M = L; Arithmetic Operations	
S_3	S_2	S_1	S_0	Logic Functions	$C_n = 0$ $C_n = 0 = L$	$C_n = 1$ $C_n = 1 = H$
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

PIN DESIGNATIONS

Designation	Pin No.	Function
$\overline{A}3, \overline{A}2, \overline{A}1, \overline{A}0$	19, 21, 23, 2	WORD A INPUTS
$\overline{B}3, \overline{B}2, \overline{B}1, \overline{B}0$	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	CARRY INPUT
M	8	MODE CONTROL INPUT
$\overline{F}3, \overline{F}2, \overline{F}1, \overline{F}0$	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	CARRY OUTPUT
$\overline{G}$	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND



12-0321


S3
S2
S1
S0
B̄3
Ā3
B̄2
Ā2
B̄1
Ā1
B̄0
Ā0
M
Cn
Ḡ
Cn +4
P̄
F̄3
F̄2
A=B
F̄1
F̄0
12-0320

A.15 74182 LOOK-AHEAD CARRY GENERATOR

Equations:

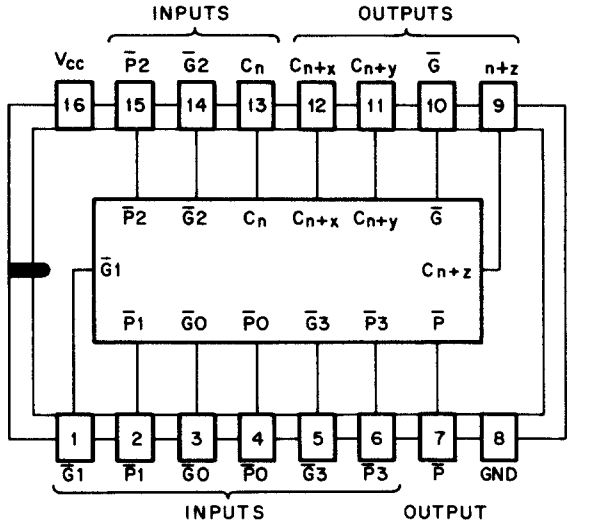
$$C_{n+x} = G_0 + P_0C_n$$

$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$

$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

$$\overline{G} = G_3 + P_3G_1 + P_3P_2G_1 + P_3P_2P_1G_0$$

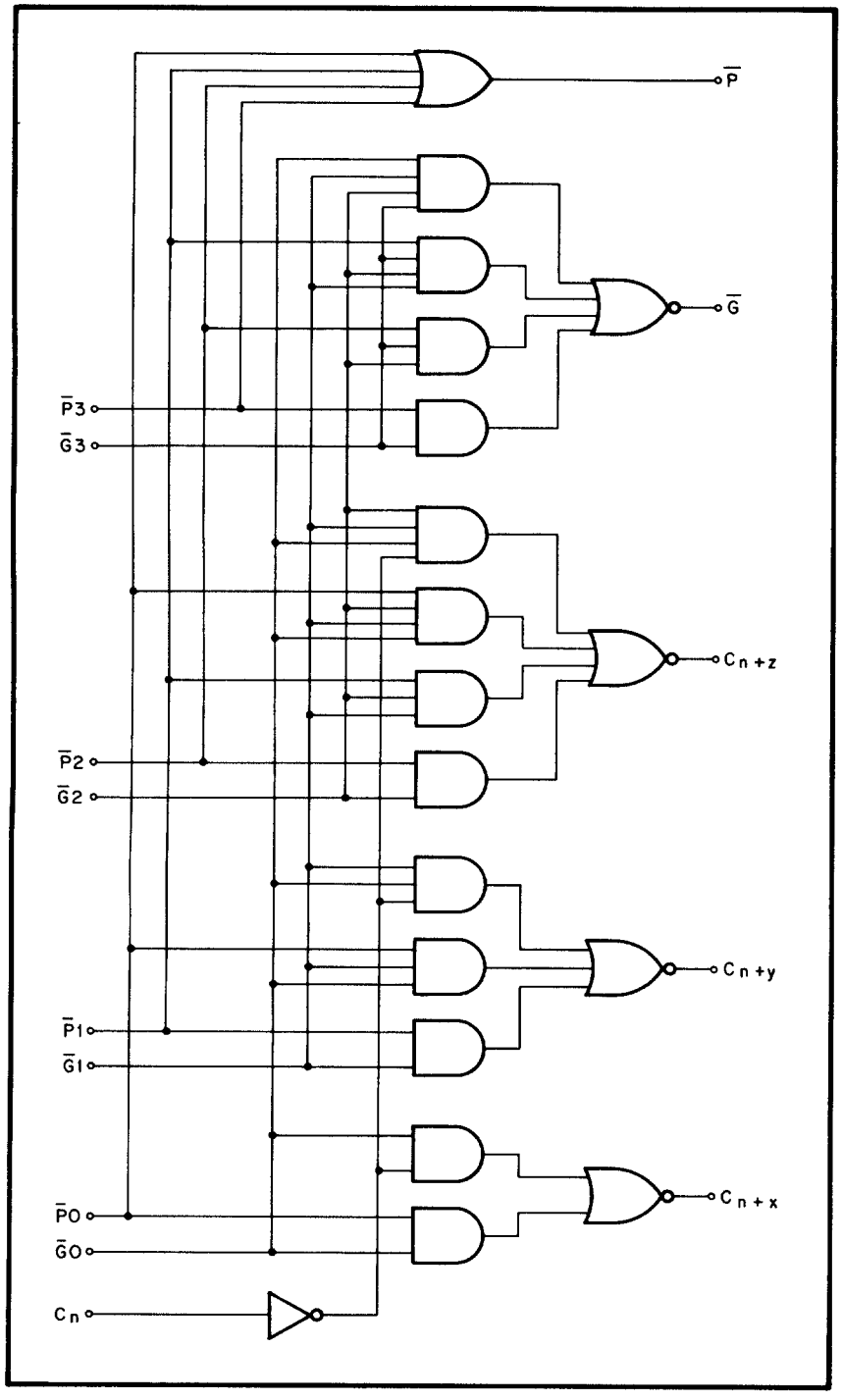
$$\overline{P} = P_3P_2P_1P_0$$



12-0326

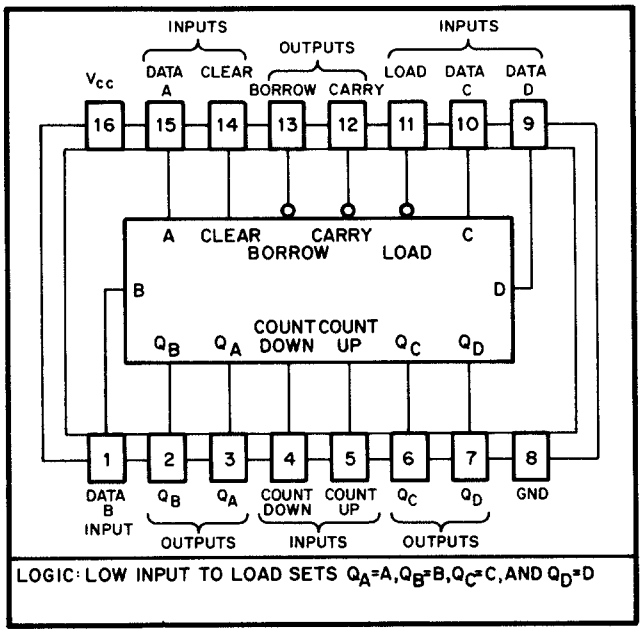
PIN DESIGNATIONS

Designation	Pin No.	Function
$\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3$	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
$\overline{P}0, \overline{P}1, \overline{P}2, \overline{P}3$	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	CARRY OUTPUTS
$\overline{G}$	10	ACTIVE-LOW CARRY GENERATE OUTPUT
$\overline{P}$	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND


$\overline{P}$
$\overline{G}$
$\overline{P}3$
$\overline{G}3$
C_{n+z}
$\overline{P}2$
$\overline{G}2$
C_{n+y}
$\overline{P}1$
$\overline{G}1$
C_{n+x}
$\overline{P}0$
$\overline{G}0$
C_n
12-0323

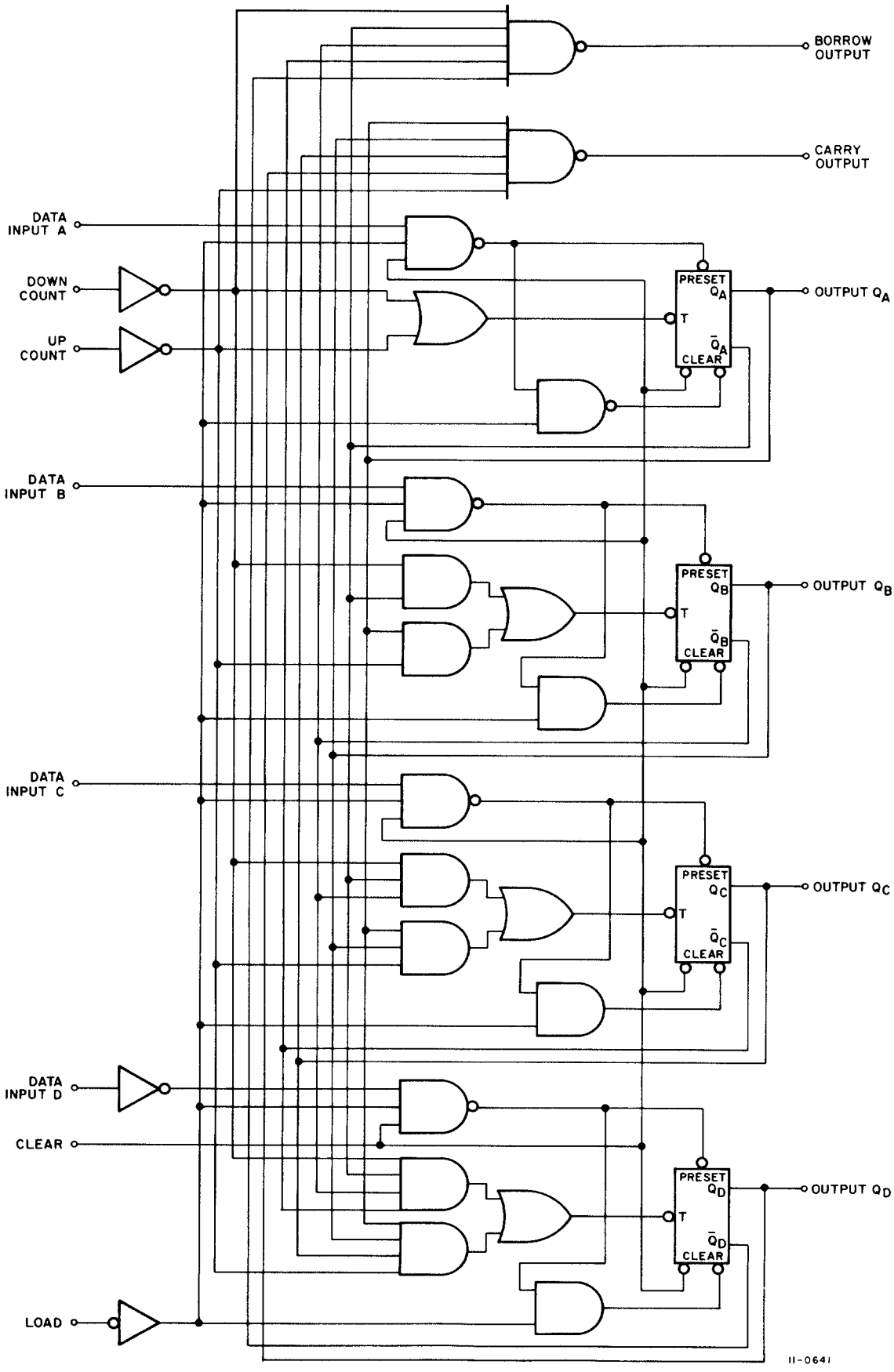
A.16 74193 SYNCHRONOUS 4-BIT UP/DOWN COUNTER (DUAL CLOCK WITH CLEAR)

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

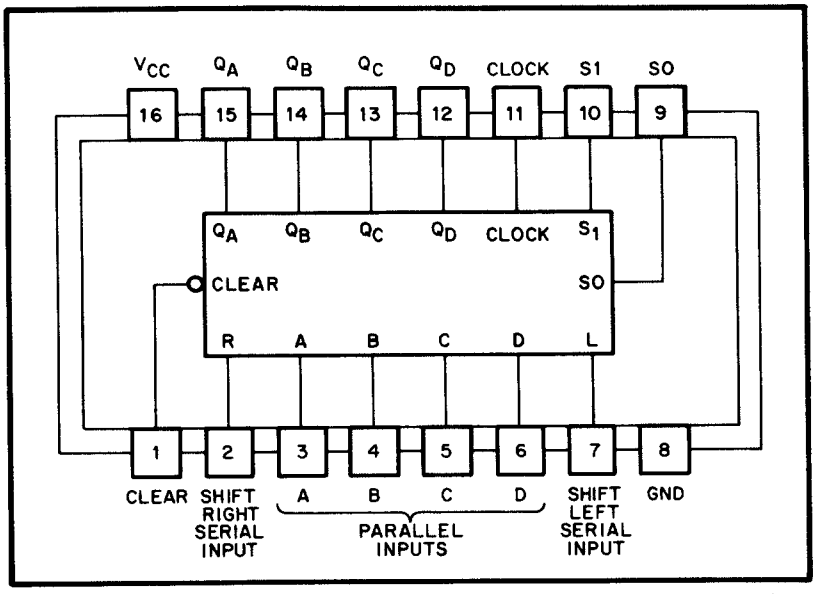


LOGIC: LOW INPUT TO LOAD SETS Q_A=A, Q_B=B, Q_C=C, AND Q_D=D

11-0640


BORROW OUTPUT
CARRY OUTPUT
DATA INPUT A
DOWN COUNT
UP COUNT
PRESET Q_A
T
$\bar{Q}_A$
CLEAR
OUTPUT Q_A
DATA INPUT B
PRESET Q_B
T
$\bar{Q}_B$
CLEAR
OUTPUT Q_B
DATA INPUT C
PRESET Q_C
T
$\bar{Q}_C$
CLEAR
OUTPUT Q_C
DATA INPUT D
CLEAR
PRESET Q_D
T
$\bar{Q}_D$
CLEAR
OUTPUT Q_D
LOAD
11-0641

A.17 74194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



11-1121

A.18 7528 DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

TRUTH TABLE

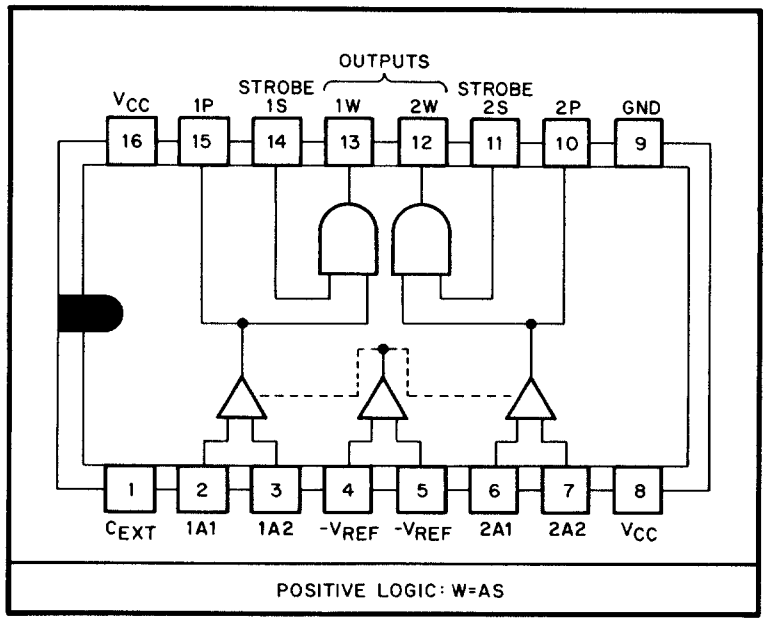
INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

11-1122

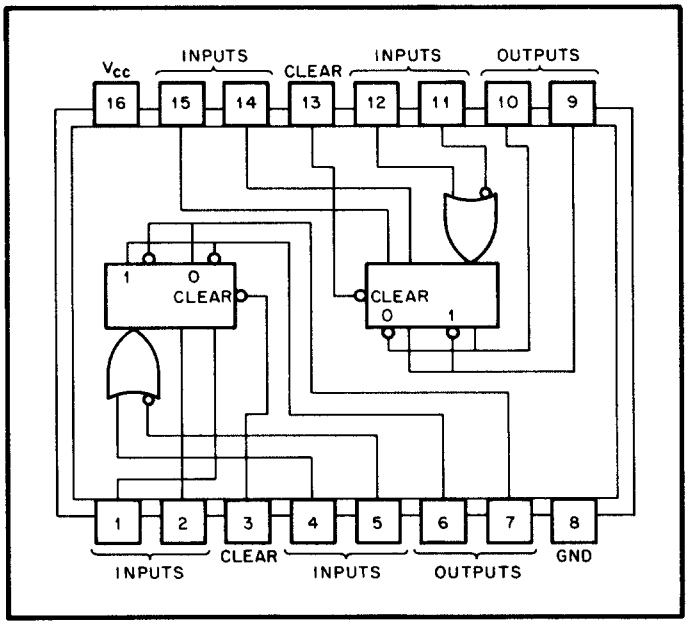
DEFINITION OF LOGIC LEVEL

INPUT	H	L	X
A†	$V_{ID} > V_T$ MAX	$V_{ID} < V_T$ MIN	IRRELEVANT
S	$V_I > V_{IH}$ MIN	$V_I < V_{IL}$ MAX	IRRELEVANT

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits V_{ID} is considered positive regardless of which terminal is positive with respect to the other.



A.19 9602 DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR



TRUTH TABLE

A	B	1	0
H	↑	⎍	⎎
↓	L	⎍	⎎

H = HIGH LEVEL
L = LOW LEVEL
↑ = LOW TO HIGH TRANSITION
↓ = HIGH TO LOW TRANSITION

11-1130

APPENDIX B
COMPUTER CONNECTORS

Table B-1 lists the computer connectors, the connector type, part number, pin and signal designations, and the associated connector cable. This includes the connectors for the SCL cable that interfaces the computer (Berg) connector to an LA30 or Model 33 ASR Teletype equivalent (Mate-N-Lok) connector. The power supply connectors are described in Part 4 of this manual.

Table B-1
Connectors

Connector	Type	Part Number	Designations		Cable
			Pin	Signals	
SCL Connector	40-pin Berg	549949 (Female) 1270090-0 (Male)	BB	-15V	70-8820
			V	SER 0+ (20 mA)	
			T	CLK IN (TTL)	
			DD	SER IN – (20 mA)	
			R	READER RUN – (20 mA)	
			N	CLK DISAB (TTL)	
			L	SER 0 – (20 mA)	
			C	+5V	
			D	SER 0 (TTL)	
			F	READER RUN + (20 mA)	
			RR	SER IN (TTL)	
			NN	20 mA INTERLOCK	
			LL	SERIAL IN + (20 mA)	
Teletype or LA30 Connector	6-pin Mate-N-Lok (Female)	1209340	2	SER 0 -	70-8360
			3	-15V	
			4	-15V	
			5	SER 0 +	
			6	READER RUN	
			7	SER IN	
Console	40-pin Berg Connector	549949 (Female) 1270090-0	PP	DAK H	BC08R-03
			BB	SW 15 (1) H	
			DD	SW 14 (1) H	
			FF	SW 13 (1) H	
			JJ	SW 12 (1) H	
			LL	SW 11 (1) H	

Table B-1 (Cont)
Connectors

Connector	Type	Part Number	Designations		Cable
			Pin	Signals	
Console (cont)			NN	SW 10 (1) H	
			RR	SW 09 (1) H	
			TT	SW 08 (1) H	
			J	SW 07 (1) H	
			L	SW 06 (1) H	
			N	SW 05 (1) H	
			R	SW 04 (1) H	
			T	SW 03 (1) H	
			V	SW 02 (1) H	
			X	SW 01 (1) H	
			Z	SW 00 (1) H	
			HH	SCAN ADRS 01 (1) L	
			KK	SCAN ADRS 02 (1) L	
			MM	SCAN ADRS 03 (1) L	
			SS	SCAN ADRS 04 (1) L	
			CC	PUP L	
			C	RUN L	
			E	KEY LOAD ADRS (1) L	
			H	KEY EXAM (1) L	
			K	KEY CONT (1) L	
			M	KEY HLT ENB (1) L	
			P	KEY START (1) L	
			S	KEY DEP (1) L	
Unibus	M920 or M930		AA1	INIT L	
			AA2	POWER (+5V)	
			AB1	INTR L	
			AB2	GROUND	
			AC1	D00 L	
			AC2	GROUND	
			AD1	D02 L	
			AD2	D01 L	
			AE1	D04 L	
			AE2	D03 L	
			AF1	D06 L	
			AF2	D05 L	
			AH1	D08 L	
			AH2	D07 L	
			AJ1	D10 L	
			AJ2	D09 L	
			AK1	D12 L	
			AK2	D11 L	
			AL1	D14 L	
			AL2	D13 L	
			AM1	PA L	
			AM2	D15 L	
			AN1	GROUND	

Table B-1 (Cont)
Connectors

Connector	Type	Part Number	Designation		Cable
			Pin	Signals	
Unibus (cont)			AN2	PBL	
			AP1	GROUND	
			AP2	BBSY L	
			AR1	GROUND	
			AR2	SACK L	
			AS1	GROUND	
			AS2	NPR L	
			AT1	GROUND	
			AT2	BR 7 L	
			AU1	NPG H	
			AU2	BR 6 L	
			AV1	BG 7 H	
			AV2	GROUND	
			BA1	BG 6 H	
			BA2	POWER (+5V)	
			BB1	BG 5 H	
			BB2	GROUND	
			BC1	BR 5 L	
			BC2	GROUND	
			BD1	GROUND	
			BD2	BR 4 L	
			BE1	GROUND	
			BE2	BG 4 H	
			BF1	AC LO L	
			BF2	DC LO L	
			BH1	A01L	
			BH2	A00L	
			BJ1	A03L	
			BJ2	A02L	
			BK1	A05L	
			BK2	A04L	
			BL1	A07L	
			BL2	A06L	
			BM1	A09L	
			BM2	A08L	
			BN1	A11L	
			BN2	A10L	
			BP1	A13L	
			BP2	A12L	
			BR1	A15L	
			BR2	A14L	
			BS1	A17L	
			BS2	A16L	
			BT1	GROUND	
			BT2	C1 L	
			BU1	SSYN L	

Table B-1 (Cont)
Connectors

Connector	Type	Part Number	Designation		Cable
			Pin	Signals	
Unibus (cont)			BU2	C0 L	
			BV1	MSYN L	
			BV2	GROUND	
AC Remote Power Turn-On Connector	Two 3-pin Mate-N-Loks (J6 and J7)	DEC 2-09350-03 (Plug is DEC 12-09351)	1	Power Request	Power Supply AC Cable
			2	Emergency shutdown	
			3	Ground	
Line Cord Connector	AC Line Plug				(110V) BC05H (230V) BC05J

PDP-11/05, 11/10
COMPUTER MANUAL
EK-11005-TM-003

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